Understanding Linear Regulators and Their Key Performance Parameters

Zhihong Yu, Principal Product Marketing and Application Engineering Manager

Introduction

Low-dropout regulators, commonly known as LDOs, are used extensively in a wide variety of electronic applications across many different industries. An LDO is generally perceived as a simple and inexpensive way to regulate and control an output voltage that is delivered from a higher input voltage supply. However, cost and simplicity are not the only reason for their widespread use. In fact, today's systems are getting more complex, noise sensitive and power hungry with every new design. The widespread use of switching power supplies at all power levels means that designers must spend more time avoiding noise coupling and interference, while improving system efficiency, so cost and simplicity cannot be the only driver.

For most applications, a datasheet's specifications of basic parameters are clear and easy to understand. Unfortunately, datasheets do not list the parameters for every possible circuit condition. Therefore, to make the best use of an LDO, it is necessary to understand the key performance parameters and their impact on given loads. Designers will need to determine whether the LDO is suitable for a specific load by closely analyzing the surrounding circuit conditions.

This article examines the key performance parameters of LDOs and their impact on delivering clean output voltage to the various devices inside an electronic system. We'll also discuss the factors a designer must consider in order to optimize a system, especially in noise sensitive and higher current usage areas.

How LDOs are Used in Applications

In most applications, LDOs are primarily used to isolate a sensitive load from a noisy power source. Unlike switching regulators, linear regulators dissipate power in the pass transistor or the MOSFET that is used to regulate and maintain the output voltage to the required accuracy. As a result, an LDO's power dissipation can be a significant disadvantage in terms of efficiency and can cause thermal issues. Therefore, it is important for designers to minimize LDO power dissipation to boost system efficiency and avoid any thermal complications.

LDOs are one of the oldest and most commonly used devices for voltage regulation; however, many of their key performance parameters are not so well understood or at least not utilized to their full potential. While cost is a very important factor, the use of LDOs is primarily driven by the system's power requirement and acceptable noise level of the load being powered. LDOs are also used for noise reduction, and to fix problems caused by electromagnetic interference (EMI) and PCB routing.

For very low current loads, an LDO's power dissipation is very minuscule, so they become an obvious choice for their simplicity, cost and ease of use. However, for high current loads greater than 500mA, other factors become more important and sometimes even critical. In these types of applications, it is important for system designers to look at performance parameters that grow in importance at higher current levels, such as the dropout voltage, load regulation and transient performance.

Since LDOs are a type of linear regulator, they are often compared with traditional linear regulators, especially in terms of cost. It is important to understand that the pass element is the core of an LDO, and this core and its surrounding circuits dictate the LDO's performance

Inside the LDO

An LDO comprises three basic functional elements: a reference voltage, a pass element and an error amplifier, as shown in Figure 1. During normal operation, the pass element behaves as a voltage controller current source. The pass element is driven by a compensated control signal from the error amplifier, which senses the output voltage and compares it with the reference voltage. All of these function blocks affect the LDO's performance. LDO manufacturers' datasheets always include specifications that indicate the performance of these functional elements.
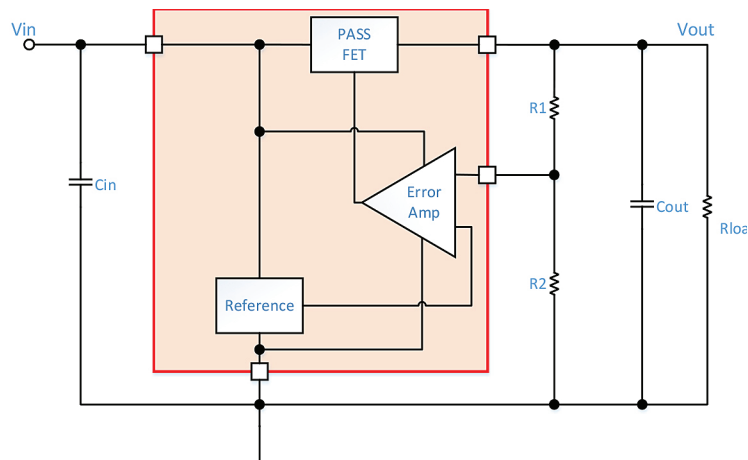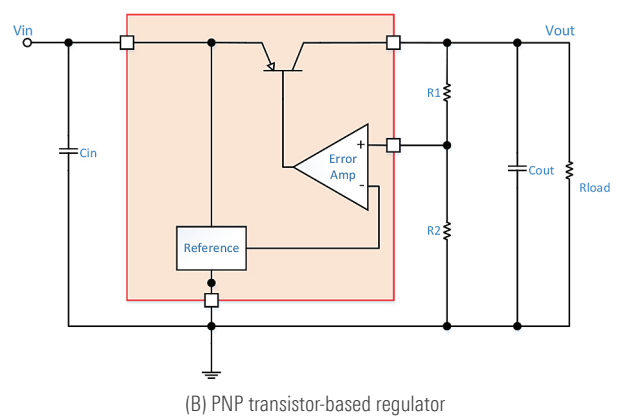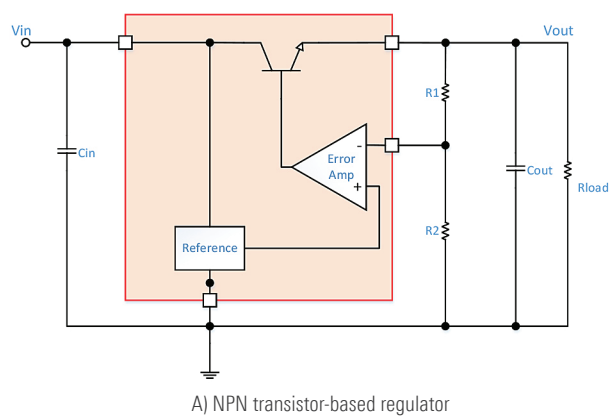
Figure 1. Block Diagram of the LDO

A) NPN transistor-based regulator

(B) PNP transistor-based regulator

(C) N-Channel MOSFET-based regulator

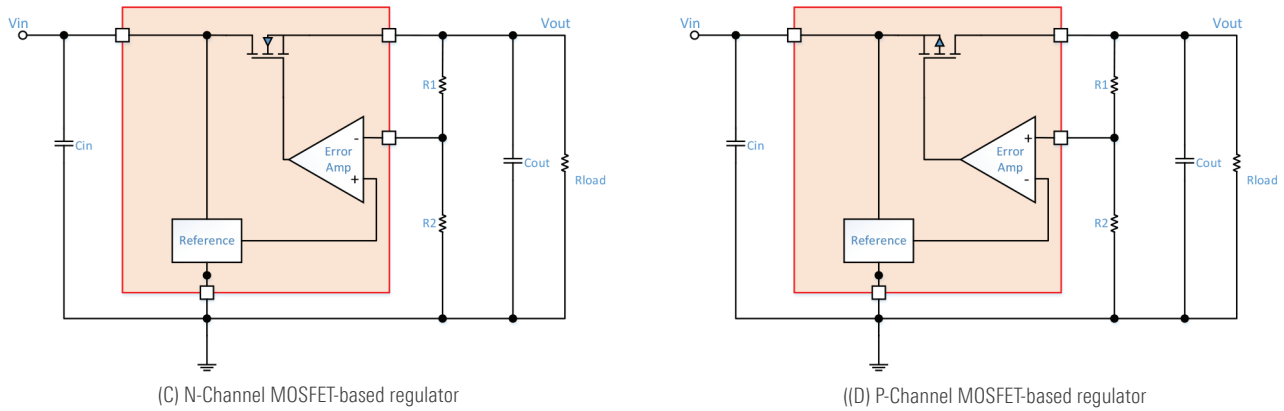((D) P-Channel MOSFET-based regulator

Figure 2. Four different types of transistors used in LDO regulators

In general, transistor-based regulators have higher dropout voltage compared to MOSFET-based regulators. Additionally, a transistor-based regulator's base driving current of the transistor pass element is proportional to the output current. This directly impacts the transistor-based regulator's quiescent current. By comparison, the MOSFET pass element uses voltage driven on the isolated gate to make its quiescent current significantly lower than the transistor-based regulator.

Key LDO Performance Parameters

1. Dropout Voltage

Dropout voltage is defined as the difference between the input and output voltages at the point when a further decrease in input voltage causes output voltage regulation to fail. In the dropout condition, the pass element operates in the linear region and behaves like a resistor. For the modern LDO, the pass element is typically implemented with PMOS or NMOS FETs, which can achieve a dropout voltage as low as 30mV to 500mV depending on loading condition. Figure 3 and 3A show the dropout voltage of RAA214020, RAA214023, RAA214220 & RAA214250 respectively. All these LDOs use PMOS FET as their pass element.
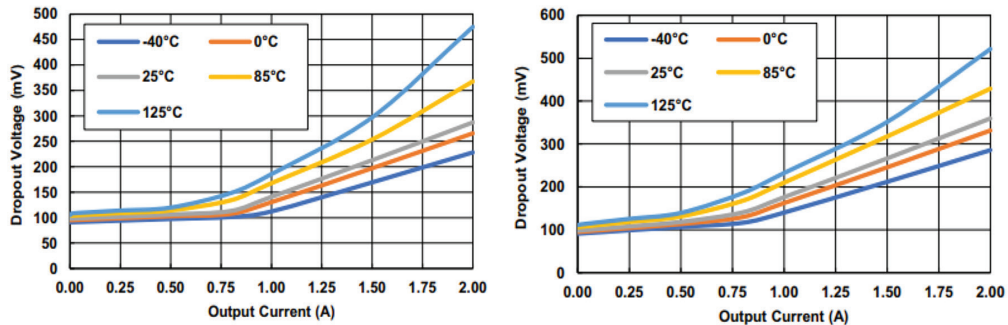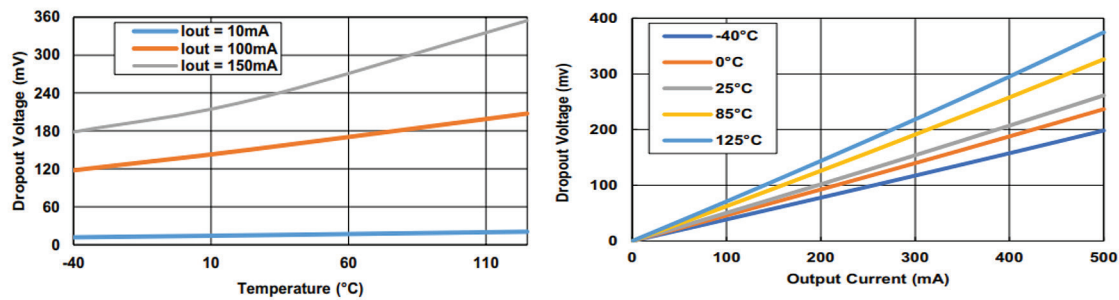

Figure 3. RAA214020 & RAA214023 dropout voltage

Figure 3A. RAA214220 and RAA214250 dropout voltage

2. Load Regulation

Load regulation is defined as the output voltage change for a given load change. This is typically from no load to full load, given by Equation 1:

$$Load\ regulation = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{V_{out@noload} - V_{out@fullload}}{0 - I_{out\_fullload}}$$

Load regulation indicates the performance of the pass element and the closed-loop DC gain of the regulator. The higher the closed-loop DC gain, the better the load regulation.

Below table shows our latest release LDOs show excellent load regulation spec.

	Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
RAA214250	Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 5V, I_{OUT} = 100µA to 500mA		0.0002		%/mA
RAA214220	Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 5V, I_{OUT} = 100uA to 150mA		0.0033		%/mA
RAA214401	Load Regulation	DV_{OUT}	0.1mA to 150mA		0.0003	0.005	%/mA
RAA214020	Load Regulation		I_{OUT} = 1mA to 2A		1		mV
RAA214023	Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10mA to 2A		0.03		%/A

3. Line Regulation

Line regulation is the output voltage change for a given input voltage change, as defined in Equation 2:

$$Line\ regulation = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{V_{out@Vin\_max} - V_{out@Vin\_min}}{V_{in\_max} - V_{in\_min}}$$

Since line regulation is also dependent on the performance of the pass element and closed-loop DC gain, dropout operation is often not included when considering line regulation. Hence, the minimum input voltage for line regulation must be higher than the dropout voltage.

Table show our latest release LDOs line regulation spec.

	Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
RAA214250	Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{IN} = V_{OUT}+1V$ to 20V		0.02	**0.05**	%/V
RAA214220	Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{IN} = V_{OUT}+1V$ to 20V		0.02	**0.05**	%/V
RAA214401	Line Regulation	DV_{OUT}	$4.5V \leq V_{IN} \leq 40V$, $I_{OUT} = 1mA$		0.0025	0.006	%/V
RAA214020	Line Regulation		$V_{IN} = 2.7V$ to 5.5V, $I_{OUT} = 1mA$		0.1		%/V
RAA214023	Line Regulation		$V_{IN} = 2.7V$ to 5.5V, $I_{OUT} = 5mA$		0.1		%/V

4. Power Supply Rejection Ratio (PSRR)

PSRR is an indication of the LDO's ability to attenuate fluctuations in the output voltage caused by the input voltage, as expressed in Equation 3. While line regulation is only considered at DC, PSRR must be considered over a wide frequency range. Equation 3:

$$PSRR = 20\,log_{10}\frac{V_{in}}{V_{out}}$$

Considered a conventional closed-loop system, the small-signal output voltage, ~Vout, can be expressed as shown in Equation 4:

$$\tilde{V}_{out} = \frac{G_{vg}}{1 + k_v \times G_C \times G_{oc}}\tilde{V}_{in} + \frac{G_C \times G_{oc}}{1 + k_v \times G_C \times G_{oc}}\tilde{V}_{ref}$$

Where ~Vin is the small signal input voltage, Gvg is the open-loop transfer function from input to output voltage, Kv is the output voltage sensing gain, Gc is the compensator's transfer function, Goc is the open-loop transfer function from the control signal to the output voltage, and $Kv \times Gc \times Goc$ is the closed-loop transfer function, $T(s)$.

As we can see in Equations 3 and 4, it is clear that the PSRR consists of the closed-loop gain, $T(s)$, and the inverse of the open-loop transfer function from input to output voltage, 1/Gvg, as shown in Figure 4. While the closed-loop transfer function dominates at lower frequencies, the open-loop transfer function from input to output voltage dominates at higher frequencies.
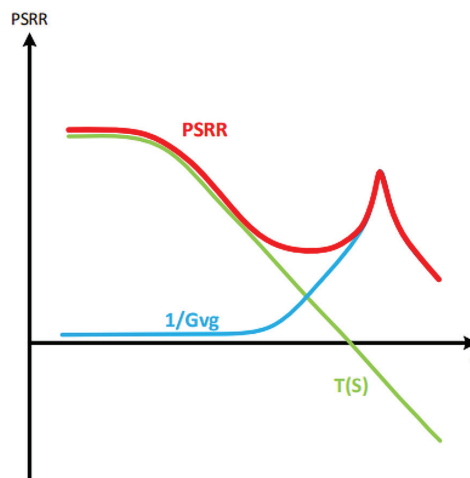

Figure 4. PSRR vs. Frequency

Below table shows our latest LDOs PSRR performance spec. Notice our high PSRR LDOs (RAA214020 and 23) are able to maintain a flat PSRR response over 100Hz~10kHz range while the others taper off. Because RAA214020/23 are design to power noise sensitive application like RF block, it is critical to use LDOs of high PSRR to minimize any possible power sources disturbance that might impact RF performance that operate over wide frequency ranges.

	Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
RAA214250	Power Supply Rejection Ratio	PSRR	FREQ = 100Hz, V_{RIPPLE} = 1V_{P-P}, I_{OUT} = 50mA, V_{IN} = 6V, V_{OUT} = 5V		87		dB
			FREQ = 10kHz, $V_{RIPPLE\ =\ 200mVP-P}$, I_{OUT} = 50mA, V_{IN} = 6V, V_{OUT} = 5V		63		dB
RAA214220	Power Supply Rejection Ratio	PSRR	f = 100Hz, I_{OUT} =10mA, V_{IN} = 6V, V_{OUT} = 5V		92		dB
			f = 10kHz, I_{OUT} = 10mA, V_{IN} = 6V, V_{OUT} = 5V		63		dB
RAA214401	Power Supply Rejection Ratio	PSRR	FREQ = 100Hz, I_{OUT} = 1mA , V_{IN} = 6V, V_{OUT} = 3.3V		74		dB
			FREQ = 10kHz, I_{OUT} = 1mA , V_{IN} = 6V, V_{OUT} = 3.3V		42		dB
RAA214020	Power Supply Rejection Ratio	PSRR	FREQ =120Hz, V_{RIPPLE} =500mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		81		dB
			FREQ = 10kHz, V_{RIPPLE} = 150mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		80		dB
			FREQ = 100kHz, V_{RIPPLE} = 150mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		64		dB
			FREQ = 1MHz, V_{RIPPLE} = 150mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		50		dB
RAA214023	Power Supply Rejection Ratio	PSRR	FREQ =120Hz, V_{RIPPLE} =500mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		84		dB
			FREQ = 10kHz, V_{RIPPLE} = 150mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		81		dB
			FREQ = 100kHz, V_{RIPPLE} = 150mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		64		dB
			FREQ = 1MHz, V_{RIPPLE} = 150mV_{P-P}, I_{OUT} = 2A, V_{IN} = 5V, V_{OUT} = 3.3V		52		dB

5. Noise

This parameter normally refers to the noise on the output voltage generated by the LDO itself, which is an inherent characteristic of the bandgap voltage reference. Equation 4 shows the relation of the reference voltage to the output voltage. Unfortunately, the closed-loop transfer function is not effective at rejecting the noise from the reference voltage to the output voltage. Hence, most low-noise LDOs need an additional filter to prevent noise from entering the closed-loop.

When you compare the pin-outs of ultra-low noise high PSRR LDOs like RAA214020/23 vs generic LDOs, you will notice an additional Cset pin is available and a smaller capacitor can be included between this pin and IC ground to optimize the output noise and PSRR performance. This small capacitor filters the noise on the LDO's bandgap – where it is most sensitive to noise.

Notice generic LDOs like RAA214220 / RAA214250 / RAA214401 only specify output RMS noise and usually they are in the >100uVrms range while ultra-low noise LDO like RAA214020/23 will include noise spectral density (i.e. nV/√(Hz)) with below 10uVrms output rms noise performance.

6. Transient Response

LDOs are commonly used in applications where point-of-load regulation is important, such as powering digital ICs, DSPs, FPGAs and low-power CPUs. The load in such applications has multiple modes of operation, which require different supply currents. As a result, the LDO has to respond quickly to keep the supply voltage within the required limits. This makes the transient behavior of an LDO one of the critical performance parameters.

As in all closed-loop systems, the transient response mainly depends on the bandwidth of the closed-loop transfer function. To achieve the best transient response, the closed-loop bandwidth has to be as high as possible while ensuring sufficient phase margin to maintain stability.

ISL80510 has excellent load transient response with relatively good output noise voltage (75uVrms) but its follow-up RAA214020/23 are designed with similar load transient response beside offering very high PSRR and ultra-low noise spectral density performance.
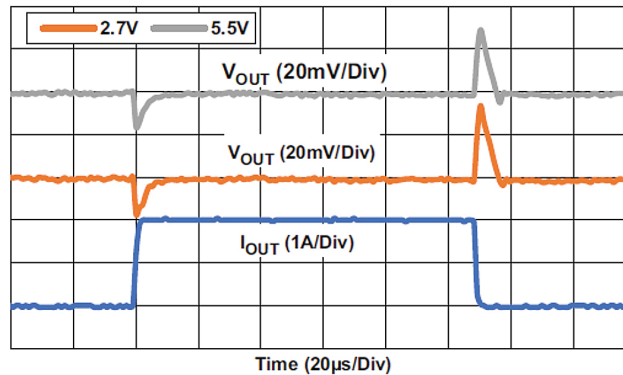
Figure 5. RAA214020 transient response (2.7Vin & 5.5Vin, 1.8Vout, ΔIOUT = 100mA to 2A at 2A/μs)

7. Quiescent Current

The quiescent current (or ground current) of an LDO is the combination of the bias current and drive current of the pass element, and is normally kept as low as possible. Additionally, when PMOS or NMOS FETs are used as the pass element, the quiescent current is relatively unaffected by the load current. Since the quiescent current doesn't pass through to the output, it influences the LDO's efficiency, which can be calculated as follows in Equation 5:

$$Efficiency = \frac{I_{out} \times V_{out}}{(I_{out} + I_q) \times V_{in}}$$

The power dissipation inside the LDO is defined by: $V_{in} \times (I_q + I_{out}) - V_{out} \times I_{out}$. To optimize the LDO's efficiency, both quiescent current and the difference between the input and output voltages must be minimized. The difference between the input and output voltages have a direct impact on efficiency and power dissipation, so the lowest dropout voltage is generally preferred.

Even though an LDO cannot deliver high efficiency conversion compared to a switching-mode power supply (SMPS), it is still a necessary voltage regulator for many modern applications. In noise sensitive applications, it is very challenging for an SMPS to achieve the necessary output ripple to meet a tight noise specification. Consequently, it is not uncommon for an LDO to be added as an active filter to the output of an SMPS. This LDO must have high PSRR at the SMPS switching frequency.

LDOs are particularly suited to applications that require an output voltage regulated to slightly below the input voltage. While buck and boost converters have limitations on the maximum/minimum duty cycle, their output voltage will lose regulation with an input voltage that is close to the output voltage.

RAA214401 is developed with the above design understanding in mind to offer customers a simple to use wide Vin range (up to 40V) 150mA LDO with ultra-low 3.6uA quiescent current and fix commonly used 3V3 output source that is well suitable to power any "always on" housekeeping MCU without implicate any major power lost concern.

RAA214220 (150mA) and RAA214250 (500mA) are developed to address 2.5V~20V input operating systems offering design flexibility to adjust Vout between 1.224V to 18V with low dropout voltage not exceeding 300mV (typ) at max loading condition. They also include enable pin when disabled only consumed <6uA quiescent current. They are perfect power companion for Renesas RA, RL78, and RX family MCUs.

Conclusion

Though simple in concept and implementation, widely used LDOs perform a vital function in system power design. There are many factors that need to be considered to optimize a design, particularly at higher current levels.

RAA214020/23 is very suited for mid- to high-current and especially to power noise sensitive applications.

RAA214401 come in a cost-effective industry compatible SOT23-3 footprint allow customers to replace conventional wide Vin to fixed 3.3Vout 150mA LDO where ultra-low quiescent current is required (e.g. sensors system, smart-metering, always-on battery-powered equipment like power-tool or vacuum, etc).

RAA214220/50 are optimized to support 2.5V~20V input operating system with excellent line and load regulation well suited to power industry leading Renesas's RA, RL78, and RX family MCUs.

Next Steps

Learn more about
- Ultra-low noise high PSRR LDOs RAA214020 & RAA214023
- Wide Vin fixed 3.3Vout micropower LDO RAA214401
- Up to 20Vin 150mA and 500mA generic LDOs RAA214220 & RAA214250

Watch the video
- Ultra-Low Noise LDOs for Sensitive Loads

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