Lecture notes of

BCS-203

COMPUTER ORGANIZATION (3-1-0)

Text Books:

1. **Computer Organization , Hamacher, TMH**
2. **Computer System Architecture, Morris Mano, PHI**

Reference Books:

1. **Computer Architecture & Organization, William Stallings, Pearson**

Prerequisite

1. **Knowledge of digital circuit**
2. **Functionality of various gates**
3. **Number System**

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Syllabus:

4TH SEMESTER B.Tech. (CSE, IT)

F.M.70

BCS-203 **COMPUTER ORGANIZATION –1 (3-1-0) Cr.-4**

Introduction: **(**05 Period)

Basic Organization of Computers, Classification Micro, Mini, Mainframe and Super Computer. System Bus and Interconnection, PCI, Computer Function, I-Cycle, Interrupt and Class of Interrupts, Von-Neumann M/c: Structure of IAS.

CPU Organization: (05 Period)

Fundamental Concepts: Fetching and storing a word in Memory, Register Transfer, Performing an Arithmetic & Logic Operation, Execution of a Completes, Branching.

General Register Organization: (15 Period)

Control word, Examples of Microsoft, Stack Organisation, Register Stack, Memory Stack, RPN, Ecaluation of Arithmetic Expression using RPN, Instruction Format: Three Address, Two Address, One Address and Zero Address Instruction, Addressing Modes: Types of Addressing modes, Numerical Examples, Program Relocation, Compaction, Data Transfer & Manipulation: Data transfer, Data Manipulation, Arithmetic, Logical & Bit Manipulation Instruction, Program Control: Conditional Branch Instruction, Subroutine, Program Interrupt, Types of Interrupt, RISC & CISC Characteristic. Control Unit Operation: Hardware Control & Micro Programmed Control.

Input/Output Organization: (10 Period)

Peripheral Devices, Input – output Interface, I/O Bus, Interface Module, Asynchronous Data Transfer, Strobe Control, Handshaking, Asynchronous Serial Transfer, Asynchronous Communication Interface, Modes of Transfer: Programmed I/O, Interrupt Driven I/O, Direct Memory Access (DMA), DMA Controller, I/O Channel & Processor.

Priority Interrupt: Daisy Chaining Priority, Parallel Priority Interrupt.

Memory Organization: (15 Period)

Computers Memory System Overview, Characteristics of Memory System, The Memory Hierarchy, Semi Conductor Main Memory types, Organisation, Memory cell Operation.

Cache Memory: Cache Principles, Elements of Cache Design, Cache Size, Mapping function, Replacement Algorithm, LRU, FIFO, LFU, Write policy. Number of Caches: Single versus two level caches, Pentium Cache Organisation. Associative Memory: Hardware Organisation, Match Logic. Read Operation, Write Operation, Auxiliary Memory: Magnetic Disks, Magnetic Tape. Virtual Memory: Paging, Paging h/w, Address Mapping using pages, Segmentation h/w, Demand Paging, Memory Management h/w.

Text Books:

1. Computer Organization & Architecture – William Stallings, 4th Edition, PHI
2. Computer System Architecture : Morris Mano, 3rd Edition, PHI

Reference Books:

1. Computer Organization – by V.Carl Hamacher, Z.G.Vranesic, and S.G.Zaky, 3rd Edition. McGraw Hill,
2. Computer Architecture and Organization, by - John P. Hayes, 3rd Edition, Mc Graw Hill International Editions.
3. Computer Organization & Design, (3rd Edition) by – D.A.Patterson & J.L.Hennessy – Morgan Kaufmann Publishers (Elseviers)

Module-I

Introduction:

What is a computer?

- A machine for high end computation. An extended size of a calculator.
- It can be analog, if it processes data in form of analog devices and digital, if processes data in form of digital signal.

Why to use computer?

Applications of a computer :

Computer is used in business organisations for:

- Payroll calculations
- Budgeting
- Sales analysis
- Financial forecasting
- Managing employees database
- Maintenance of stocks etc.

Today banking is almost totally dependent on computer.

- Banks provide online accounting facility, which includes current balances, deposits, overdrafts, interest charges, shares, and trustee records.
- ATM machines are making it even easier for customers to deal with banks.

The computer has provided a lot of facilities in the education system.

- The computer provides a tool in the education system known as CBE (Computer Based Education).
- CBE involves control, delivery, and evaluation of learning.
- The computer education is rapidly increasing the graph of number of computer students.

- There are number of methods in which educational institutions can use computer to educate the students.
- It is used to prepare a database about performance of a student and analysis is carried out on this basis.

In marketing, uses of computer are following:

- Advertising **-** With computers, advertising professionals create art and graphics, write and revise copy, and print and disseminate ads with the goal of selling more products.
- At Home Shopping **-** Home shopping has been made possible through use of computerised catalogues that provide access to product information and permit direct entry of orders to be filled by the customers.

Computers are widely used in Engineering purpose.

One of major areas is CAD (Computer aided design). That provides creation and modification of images. Some fields are:

- Structural Engineering **-** Requires stress and strain analysis for design of Ships, Buildings, Budgets, Airplanes etc.
- Industrial Engineering **-** Computers deal with design, implementation and improvement of integrated systems of people, materials and equipments.
- Architectural Engineering **-** Computers help in planning towns, designing buildings, determining a range of buildings on a site using both 2D and 3D drawings.

Computers are largely used in defense:

Modern tanks, missiles, weapons etc. Military also employs computerised control systems. Some military areas where a computer has been used are:

- Missile Control
- Military Communication

- Military Operation and Planning
- Smart Weapons

Communication:

means to convey a message, an idea, a picture or speech that is received and understood clearly and correctly by the person for whom it is meant for. Some main areas in this category are:

- E-mail
- Chatting
- Usenet
- FTP
- Telnet

Video-conferencing

Computers play an important role in government:

- Budgets
- Sales tax department
- Income tax department
- Male/Female ratio
- Computerization of voters lists
- Computerization of driving licensing system
- Computerization of PAN card

Units of a Computer system:

- To provide the information to be computed and interacting purpose (Input Unit: Like Monitor, Mouse, Joystick etc.)
- To compute and control the whole system (CPU : CO +ALU)
- To get & sense the result (Output Unit: Like Monitor, Printer, Micro phones, speakers etc)

- To store the information for future referencing (Memory: Like Hard disc, flash memory, magnetic tape, ROM, RAM etc.)

Block diagram of a computer

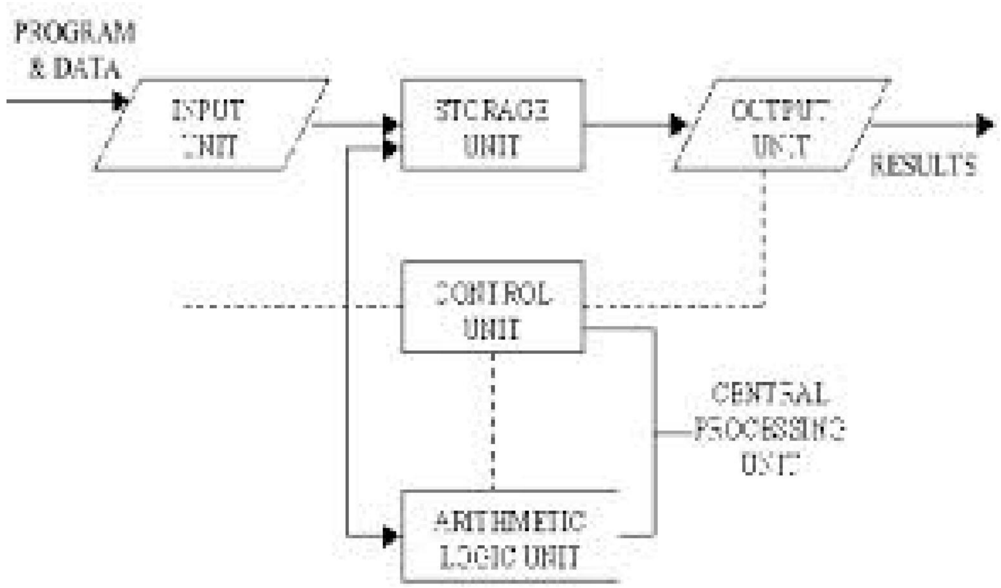


Fig:1: Block Diagram of a Computer

Structure

- Simplest possible view of a computer show in figure 1:

  o Storage

  o Processing

  o Peripherals

  o Communication Lines

Brief History of Computers

1. First Generation: Vacuum Tubes

- 1943-1946: ENIAC

- first general purpose computer designed by Mauchly and Eckert.
- The ENIAC was a decimal rather than a binary machine. That is, numbers were represented in decimal form, and arithmetic was performed in the decimal system. Its memory consisted of 20 “accumulators” each capable of holding a 10-digit decimal number. A ring of 10 vacuum tubes represented each digit. At any time, only one vacuum tube was in the ON state, representing one of the 10 digits. The major drawback of the ENIAC was that it had tube programmed manually by setting switches and plugging and unplugging cables.
- The first task was to perform series of complex calculation that is helped determine Hydrogen-bomb feasibility instead. General purpose use only.
- It can process 30 tons + 15000 sq. ft. + 18000 vacuum tubes + 140 KW = 5000 additions/sec

Vvon Neumann Machine

1945: stored-program concept first implement for EDVAC. Key concepts:

- Data to be processed and instructions to b executed on those data are stored in a single read-write memory
- The contents of this memory are addressable by location, without regard to the type of data contained there.
- Execution occurs in a sequential fashion (unless explicitly modified) from one instruction to the next.

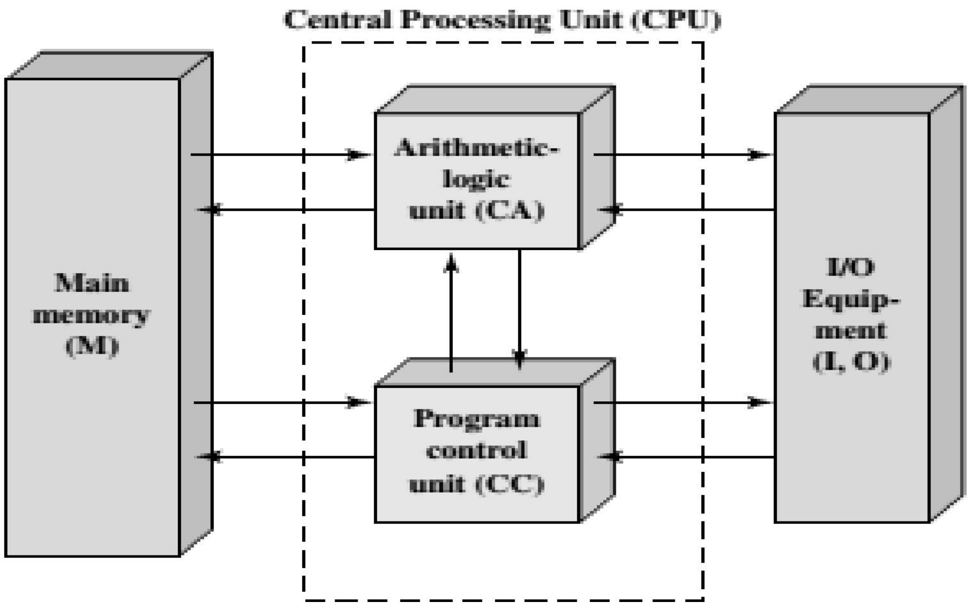
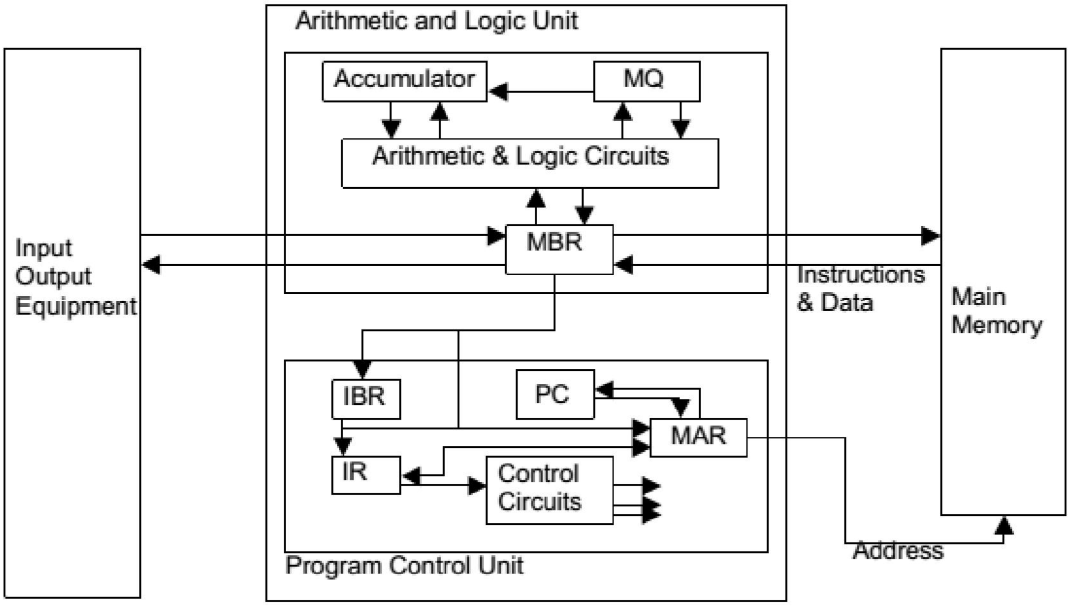

Central Processing Unit (CPU)
Main memory (M)
Arithmetic-logic unit (CA)
Program control unit (CC)
I/O Equip-ment (I, O)

Fig.2 Von Neumann Machine

Institute for Advanced Studies (IAS) computer

- In 1946 atPrinceton.
- Prototype for all subsequent general-purpose computers. With rare exceptions, all of today's computers have this same general structure, and are thus referred to as von Neumann machines like fig. 3.
- A main memory, which stores both data and instructions
- An ALU capable of operating on binary data.
- A control unit, which interprets the instructions in memory and causes them to be executed.

Fig.3: Expanded Structure of IAS Computer



First commercial computers

- 1950: UNIVAC - commissioned by Census Bureau for 1950 calculations.
- late 1950's: UNIVAC II
  - greater memory and higher performance.
  - Same basic architecture as UNIVAC
  - First example of upward compatibility
- 1953: IBM 701 - primarily for science
- 1955: IBM 702 - primarily for business

Second Generation: Transistors

- 1947: Transistor developed at Bell Labs
- Introduction of more complex ALU and control units
- High-level programming languages
- Provision of system software with computers
- The data channel – an independent I/O module with its own processor and instruction set

- The multiplexor – a central termination point for data channels, CPU, and memory. Precursor to idea of data bus.

Third Generation: Integrated Circuits

- 1958: *Integrated circuit developed*
- 1964: *Introduction of IBM System/360*
  - First planned family of computer products. Characteristics of a family:
    - Similar or Identical Instruction Set and Operating System
    - Increasing Speed
    - Increasing Number of I/O Ports
    - Increasing Memory Size
    - Increasing Cost
  - Different models could all run the same software, but with different price/performance.
- 1964: *First PDP-8 shipped*
  - First minicomputer
  - Started OEM market
  - Introduced the bus structure

Fourth Generation: No clear characterization

- Semiconductor memory
  - Replaced bulky core memory
  - Goes through its own generations in size, increasing by a factor of 4 each time: 1K, 4K, 16K, 64K, 256K, 1M, 4M, 16M on a single chip w/ declining cost and access time.
  - Microprocessors and personal computers.
- Distributed computing.
- Larger and larger scales of integration.

Classification of Computers:

Micro Computer System

These are also known as personal computers and are the ones mostly found in big and small office, they are normally standalone computers known PC, or Desktop Computers. Micro Computers are small and expensive designed for individual use. It contains two types of memories RAM and ROM.

Minicomputer systems

Mini computers are midsized computers capable of supporting from 4 – 200 users simultaneously. Mini pc are mainly used as departmental computers for data processing in large organization or governmental institutions like hospitals.

Main frame computer systems

A main frame computer is a very large expensive computer system capable of supporting hundreds and thousands of users simultaneously, most of these computers are found in large organizations like universities, hospitals, world governing body like UN among many others.

Super computer systems

Super Computers are the fastest computer which were very expensive and requires a lot of mathematical calculations. The first generation of super computer was developed by VON-Newman.

The study of digital computer has been carried out various ways with different perspective or analysis.

- **Computer Arcitecture:**

mostly it refers to those attributes of a system visible to a programmer or those attributes that have a direct impact on the logical execution of a program.

Examples of architectural attributes include:

a. instruction set designing
b. instruction format
c. no of bits used to represent various types of data
d. different addressing mechanism to access data

Computer organization :

- refers to the operational units and their interconnections that realize the architectural specifications. Organizational attributes include those hardware details transparent to the programmer, such as control signals; interfaces between the computer and peripherals; and the memory technology used and peripherals; and the memory technology used.

Ex: Two different models from a same vendor like Intel are brought to analyze. Both the models(lap top and desk top) have same processor like core 2 duo. That means both models understand the same instruction set as you know each processor understands a fixed no of instructions. Hence forth their architecture is same. Due to the placement of various hardware components, one model (laptop) is slim and other is bulky. Hence their organization is different

Bus and Interconnection:

Bus:

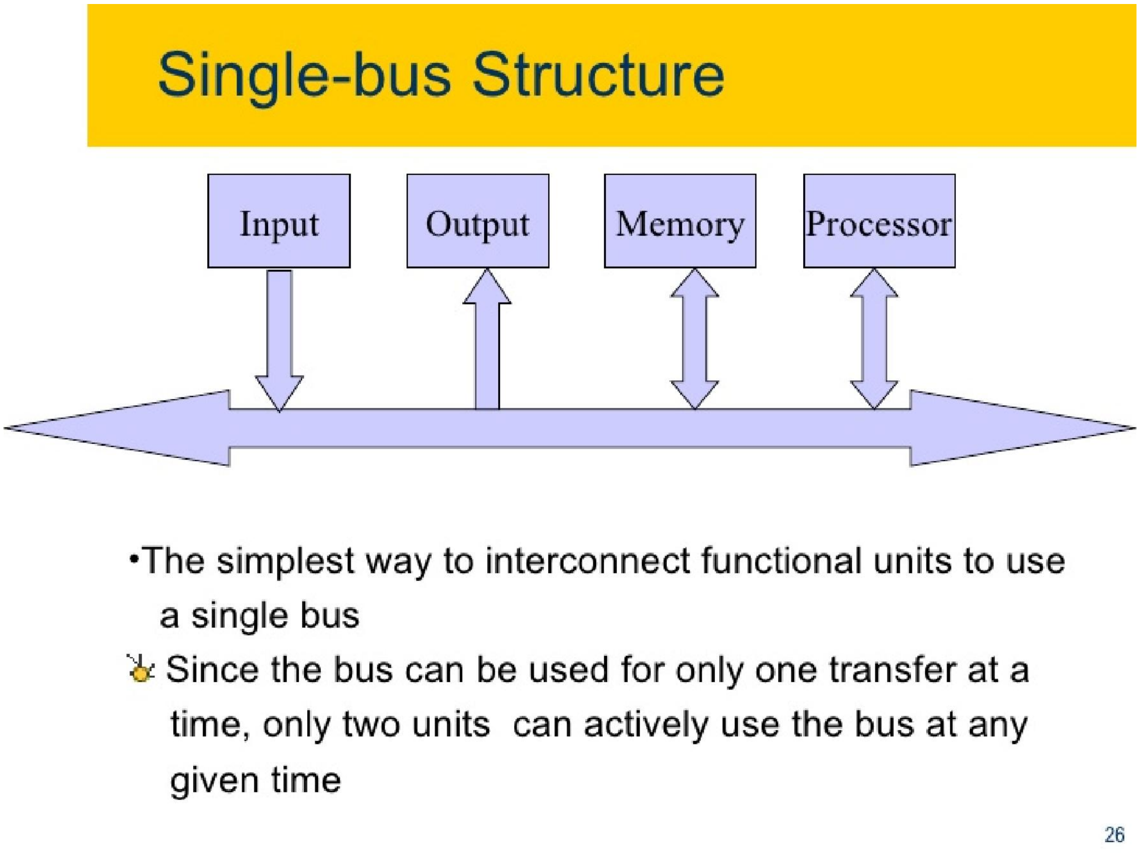
is a bunch of wires for

- connecting several components
- and communicating the signals/ information between those components.

Interconnection:

Interconnection of the components of the computers can be in two ways.

- Single bus interconnection (acc. to fig. 4)
- Multi-bus interconnection (acc. to fig. 5)



Single-bus Structure

- The simplest way to interconnect functional units to use a single bus
- Since the bus can be used for only one transfer at a time, only two units can actively use the bus at any given time

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Fig. 4 Single bus interconnection

Bus Types:

- Dedicated

- Separate data, address and control lines

- Multiplexed

- Shared lines

Dedicated

Like fig.4.

1. **Data bus:** It carries the data from one system module to other. Data bus may consist of 32,64, 128 or even more numbers of separate lines. This number of lines decides the width of the data bus. Each line can carry one bit at a time. So, a data bus with 32 lines can carry 32bit of

data at a time. If a processor needs to read 64bit of data from memory then the processor must access the memory twice.

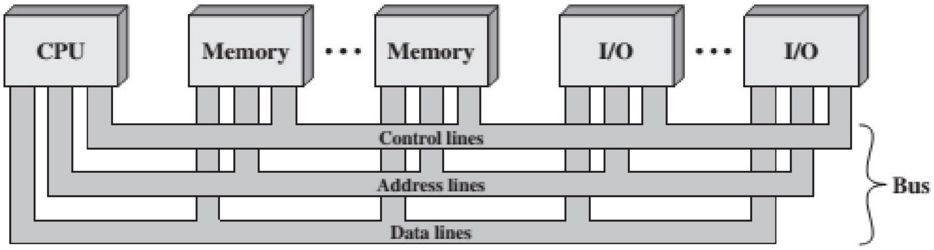


Fig. 5 Multi-Bus Interconnection

2. Address Bus: It is used to carry the address of source or destination of the data on the data bus.

3. Control Bus: It is used to control the access, processing and information transferring. As either the exclusive data and address lines are shared by all components or common paths may create congestion in traffic, there must be a separate and dedicated path for control signal transfer.

Multiplexed:

Either data or address or instruction flows through the bus like fig.6.

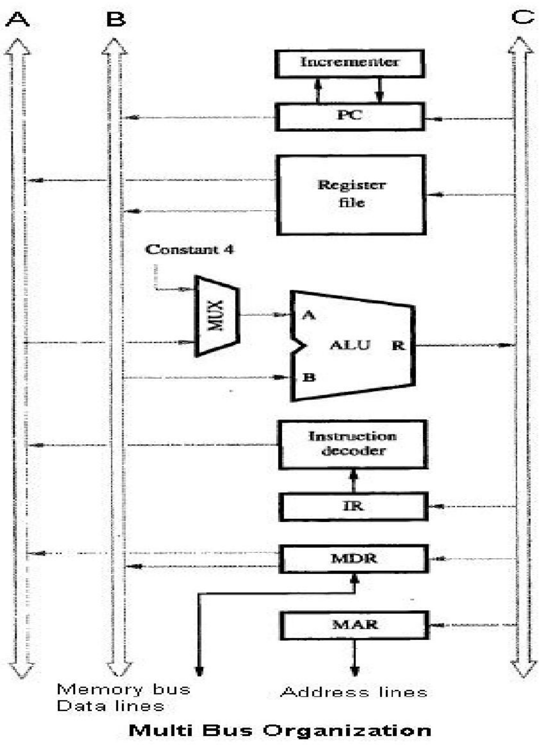


Fig.6 3 bus CPU architecture.

PCI:

PCI stands for Peripheral Component Interconnect. It is

- high bandwidth, independent bus
- used to connect peripheral devices like Graphics card, LAN card, disk controller and so on .

Bus Structure of PCI

PCI may be configured as a 32- or 64-bit bus like fig. 7 & fig.8. The 49 mandatory signal lines for PCI are divided into the following functional groups:

Ø **System pins**: Include the clock and reset pins.

Ø **Address and data pins**: Include 32 lines that are time multiplexed for addresses and data. The other lines in this group are used to interpret and validate the signal lines that carry the addresses and data.

Ø **Interface control pins**: Control the timing of transactions and provide coordination among initiators and targets.

- Ø **Arbitration pins**: Unlike the other PCI signal lines, these are not shared lines. Each PCI master has its own pair of arbitration lines that connect it directly to the PCI bus arbiter.
- Ø **Error reporting pins**: Used to report parity and other errors.

Different Bus Types of PCI

- PCI 32 bits have a bus speed of 33 MHz and operate at 132 MBps
- PCI 64 bits have a bus speed of 33 MHz and operate at 264 MBps
- PCI 64 bits have a bus speed of 66 MHz and operate at 512 MBps
- PCI 64 bits have a bus speed of 66 MHz and operate at 1 GBps.

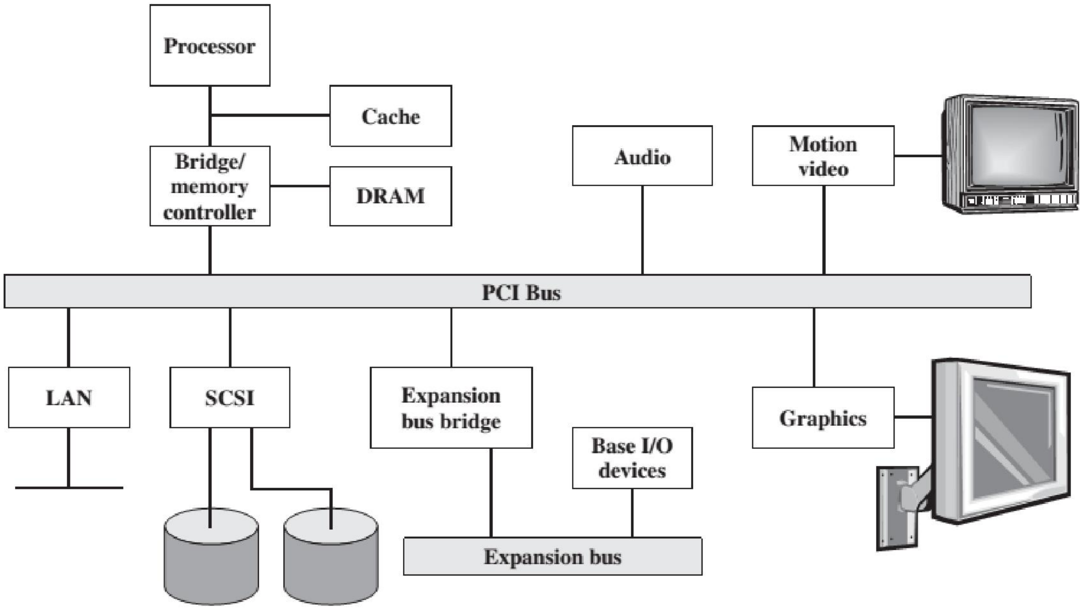


Fig.7 Typical server system

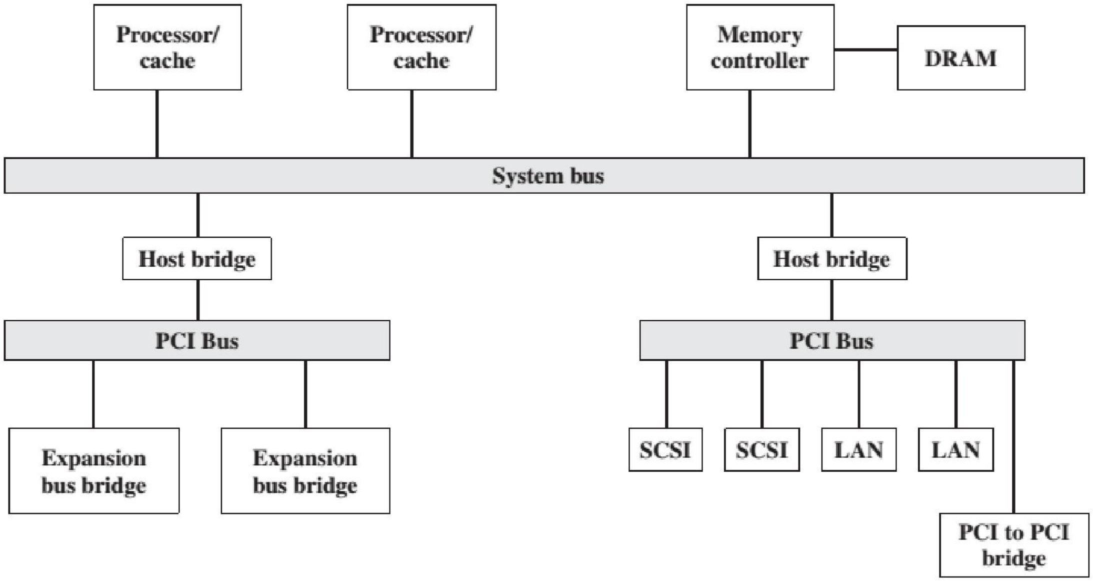


Fig.8 Typical server system

CPU Components:

- **Memory Address Register (MAR) -** Specifies address for next read or write.
- **Memory Buffer Register (MBR) –** Contains data to be written into or receives data read from memory.
- **Program Counter(PC)** -Stores the address of the next instruction to be executed.
- **General Purpose Registers(R1, R2 etc.**) -Used for storing information at the time of execution by the user.
- **Instruction Register(IR)** – Stores instruction before decoding.
- **Instruction Decoder(ID) –** Decodes the instruction before execution.
- **Arithmetic & Logic Unit(ALU)-** It does all the arithmetic and logical computations.
- **Control Unit(CU)-** Generates control signals to control every action inside the computer.

I-Cycle or Instruction Cycle

Procedure for an instruction execution one by one sequentially inside CPU is called an instruction cycle. It is divided into 2 cycles as shown in figure 9.

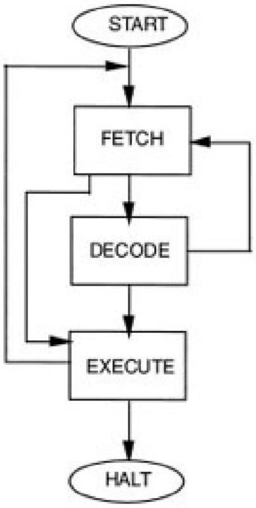


FIGURE 6 Basic instruction processing cycle.

Fig.9 Basic Instruction Cycle

- **Fetch Cycle**

  It includes certain steps like:

  1. Fetching Instruction to be executed
  2. Decoding of instruction
  3. Reading the operands to be operated

- **Execute Cycle:**

  It includes steps like:

  1. Executing or processing the operands in ALU
  2. Storing the result at the destination

Interrupt

Interrupt is mechanism of interrupting the current execution of a process.

Class of Interrupts:

Interrupts are mainly classified into following class of interrupts

1. Program Interrupt: As a result of program execution. Generated by program.

2. Timer: Generated by hardware timer.

3. I/O Interrupt: Generated by I/O devices or due to I/O error.

4. Hardware Failure.

Instruction cycle with interrupts

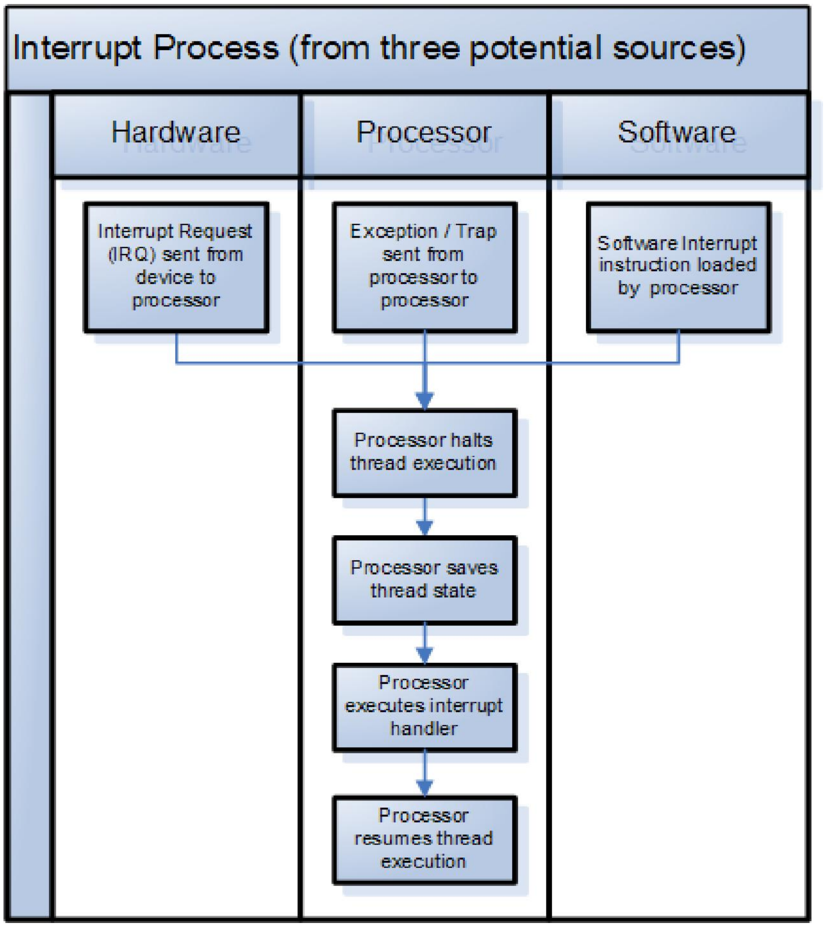

Interrupt Process (from three potential sources)
Hardware
Processor
Software
Interrupt Request (IRQ) sent from device to processor
Exception / Trap sent from processor to processor
Software Interrupt instruction loaded by processor
Processor halts thread execution
Processor saves thread state
Processor executes interrupt handler
Processor resumes thread execution

Fig.10 Instruction Cycle with Interrupts

When an interrupt signal is generated, the processor:

1. It suspends execution of the current program being executed and saves its context. This means saving the address of the next instruction to be executed (current contents of the program counter) and any other data relevant to the processor's current activity.

2. It sets the program counter to the starting address of an interrupt handler routine (Or ISR).

3. Executes the routine

4. Then interrupted program is resumed for execution.

Computer Arithmetic

1. **Data Representation:**

It is of two types.

- Fixed Representation
- Floating point Representation

Fixed Representation:

It's the representation for integers only where the decimal point is always fixed. i.e at the end of rightmost point.

it can be again represented in two ways.

1. Sign and Magnitude Representation

- In this system, he most significant (leftmost) bit in the word as a sign bit. If the sign bit is 0, the number is positive; if the sign bit is 1, the number is negative.
- The simplest form of representing sign bit is the sign magnitude representation.
- One of the draw back for sign magnitude number is addition and subtraction need to consider both sign of the numbers and their relative magnitude.
- Another drawback is there are two representation for 0(Zero) i.e +0 and -0.

2. One's Complement (1's) Representation

- In this representation negative values are obtained by complementing each bit of the corresponding positive number.

  For example 1s complement of 0101 is 1010 .
- The process of forming the 1s complement of a given number is equivalent to subtracting that number from 2^n-1 i.e from 1111 for 4 bit number.

3. Two's Complement (2's) Representation

- Forming the 2s complement of a number is done by subtracting that number from 2^n.
- So 2s complement of a number is obtained by adding 1 to 1s complement of that number.

  Ex: 2's complement of 0101 is 1010 +1 = 1011

NB: In all three systems, the leftmost bit is 0 for positive number and 1 for negative number. Figure 7 represent the three types of number representation.

Negation

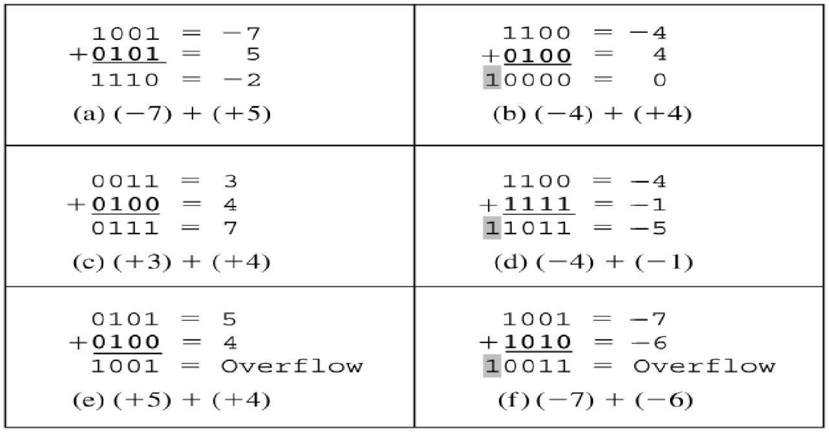
In sign-magnitude representation, the rule for forming the negation of an integer is simple: invert the sign bit. In twos complement notation, the negation of an integer can be formed with the following rules:

1. Take the Boolean complement of each bit of the integer (including the sign bit). That is, set each 1 to 0 and each 0 to 1.
2. Treating the result as an unsigned binary integer, add 1.

This two-step process is referred to as the twos complement operation, or the taking of the twos complement of an integer.

Addition:

- In addition two numbers are added like addition of +ve integers.
- On any addition, the result may be larger than can be held in the word size being used. This condition is called overflow.
- When overflow occurs, the ALU must set the overflow bit as 1 indicating the overflow.
- If two numbers are added, and they are both positive or both negative, then overflow occurs if and only if the result has the opposite sign. If one of the operand is –ve then it has to be represented in either of the complement form for getting correct result.

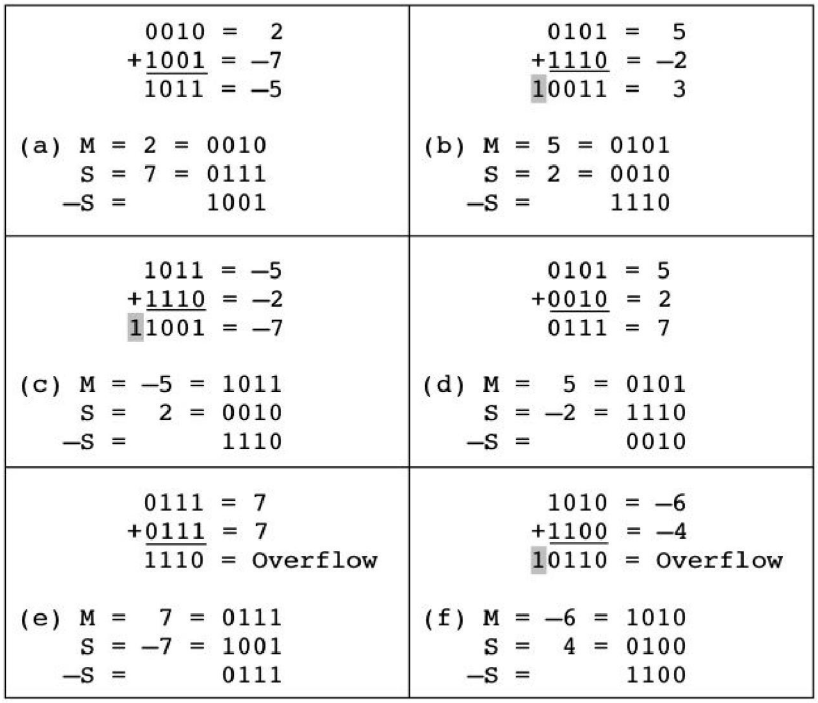


1001 = −7 +0101 = 5 1110 = −2 (a) (−7) + (+5)	1100 = −4 +0100 = 4 10000 = 0 (b) (−4) + (+4)
0011 = 3 +0100 = 4 0111 = 7 (c) (+3) + (+4)	1100 = −4 +1111 = −1 11011 = −5 (d) (−4) + (−1)
0101 = 5 +0100 = 4 1001 = Overflow (e) (+5) + (+4)	1001 = −7 +1010 = −6 10011 = Overflow (f) (−7) + (−6)

Subtraction:

- To subtract one number (subtrahend) from another (minuend), take the 2's complement (or negation) or 1's complement of the subtrahend and add it to the minuend.
- When using the complement methods in subtraction and having no additional 1 in the extreme left cell, then , this means a negative result.
- In this case, the solution is the negative of 1's complement of the result (if using 1's complement initially), or the negative of 2's complement of the result (if using 2's complement initially).
- If there is a carry in the extreme left then in 1's complement, it is discarded and 2's complement, it is added to the result.

  As examples of these operations:

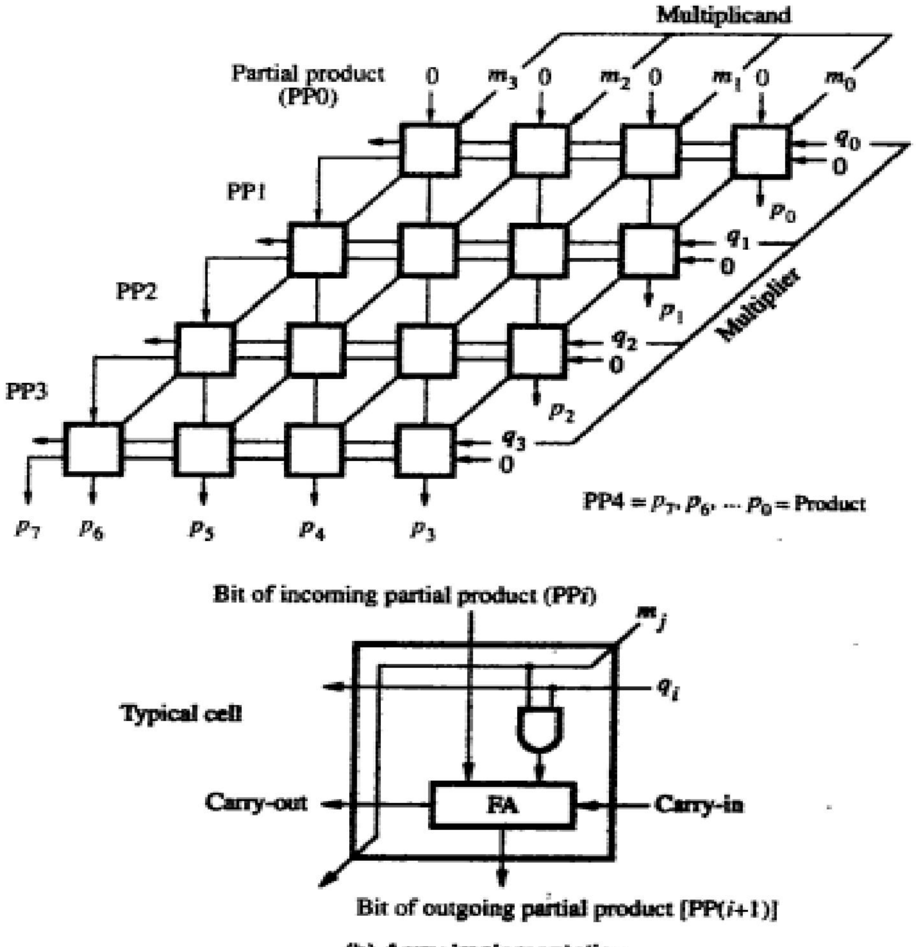


0010 = 2 +1001 = –7 1011 = –5 (a) M = 2 = 0010 S = 7 = 0111 –S = 1001	0101 = 5 +1110 = –2 10011 = 3 (b) M = 5 = 0101 S = 2 = 0010 –S = 1110
1011 = –5 +1110 = –2 11001 = –7 (c) M = –5 = 1011 S = 2 = 0010 –S = 1110	0101 = 5 +0010 = 2 0111 = 7 (d) M = 5 = 0101 S = –2 = 1110 –S = 0010
0111 = 7 +0111 = 7 1110 = Overflow (e) M = 7 = 0111 S = –7 = 1001 –S = 0111	1010 = –6 +1100 = –4 10110 = Overflow (f) M = –6 = 1010 S = 4 = 0100 –S = 1100

Multiplication Algorithm:

Multiplication of positive number **Multiplication of positive number**

- The usual way of multiplying integers is shown in figure below. The product of the two 4 bit number can be stored using 2n bits digits. So product of two 8 bit numbers is 16 bit.
- For multiplication two inputs are required i.e.
  - Multiplier Q given by Q= q_{n-1} q_{n-2}……q2 q1 q0
  - and Multiplicand M given by M= m_{n-1} m_{n-2} …….m1 m0



(b) Array implementation

Fig. 11: A 4-bit multiplier unit

Signed binary Multiplication(Booth's Algorithm)

- In this technique, two bits of the multiplier, Q(i) Q(i-1), (0<=i<=n-1), are inspected at a time.
- The action taken depends on the binary values of the two bits, such that if the two values are respectively 01, then A =A+M; if the two values are 10, then A =A-M.
- No action is needed if the values are 00 or 11.
- In all four cases, an arithmetic shift right operation on the concatenation of A Q is performed.
- The whole process is repeated n times (n is the number of bits in the multiplier).

- The Booth's algorithm requires the inclusion of a bit Q(-1)=0 as the least significant bit in the multiplier Q at the beginning of the multiplication process.
- The Booth's algorithm is illustrated in fig.12.

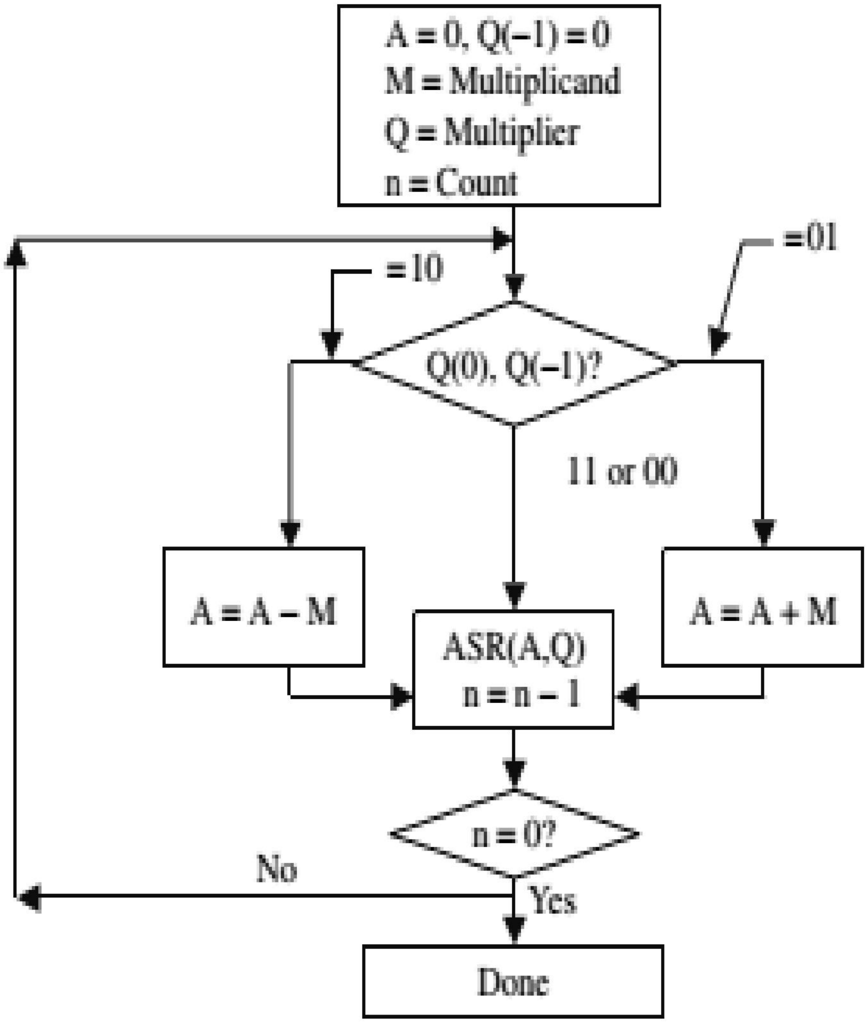


Fig.11 Booth's algorithm

Example Consider the multiplication of the two positive numbers $M = 0111$ (7) and $Q = 0011$ (3) and assuming that $n = 4$. The steps needed are tabulated below.

M	A	Q	$Q(-1)$		
0111	0000	0011	0	Initial value	
0111	1001	0011	0	$A = A - M$	
0111	1100	1001	1	ASR	End cycle #1
0111	1110	0100	1	ASR	End cycle #2
0111	0101	0100	1	$A = A + M$	
0111	0010	1010	0	ASR	End cycle #3
0111	0001	0101	1	ASR	End cycle #4
	$\underbrace{0001\ \ 0101}_{+21 \text{ (correct result)}}$				

Example Consider the multiplication of the two numbers $M = 0111$ (7) and $Q = 1101$ (−3) and assuming that $n = 4$. The steps needed are tabulated below.

M	A	Q	$Q(-1)$		
0111	0000	1101	0	Initial value	
0111	1001	1101	0	$A = A - M$	
0111	1100	1110	1	ASR	End cycle #1
0111	0011	1110	1	$A = A + M$	
0111	0001	1111	0	ASR	End cycle #2
0111	1010	1111	0	$A = A - M$	
0111	1101	0111	1	ASR	End cycle #3
0111	1110	1011	1	ASR	End cycle #4
	$\underbrace{1110\ \ 1011}_{-21 \text{ (correct result)}}$				

Division Algorithm:

Unsigned Division algorithm

- Using same registers (A,M,Q, count) as multiplication
- Results of division are quotient and remainder
- Q will hold the quotient
- A will hold the remainder
- Initial values — Q =0
- A ß Dividend
- M ß - Divisor
- Count ß n

Signed Division algorithm

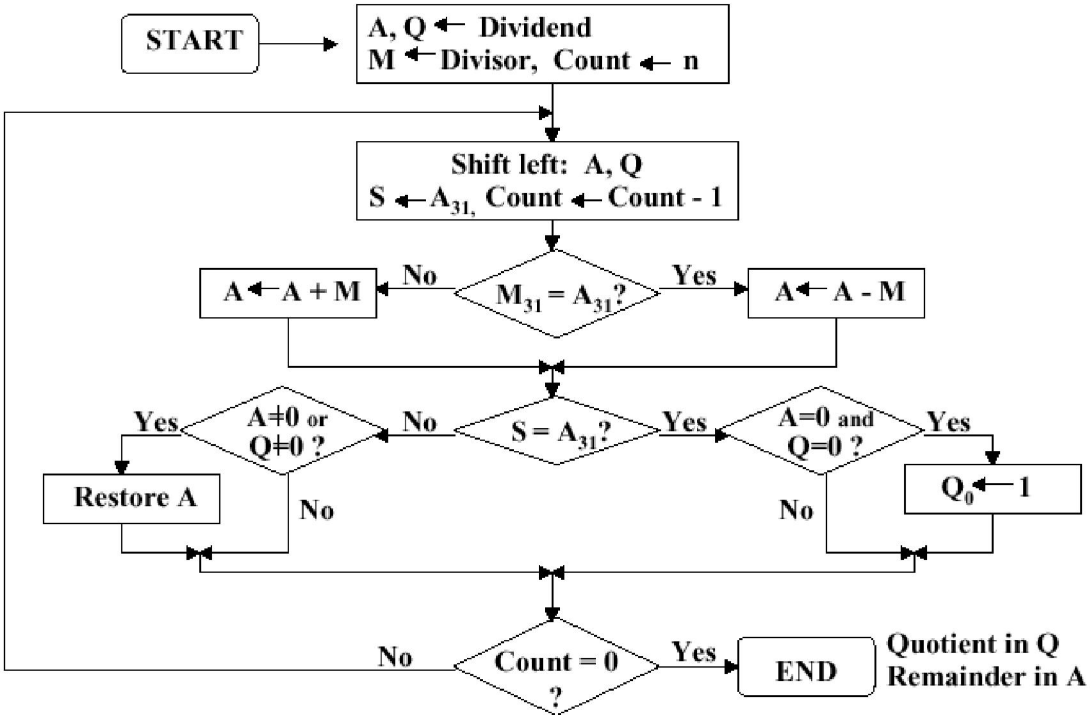


Fig. 13 Division algorithm

A	Q	M = 0011	
0000	0111	Initial values	
0000	1110	Shift	1
1101		Subtract	
0000	1110	Restore	
0001	1100	Shift	2
1110		Subtract	
0001	1100	Restore	
0011	1000	Shift	3
0000		Subtract	
0000	1001	$Q_0 = 1$	
0001	0010	Shift	4
1110		Subtract	
0001	0010	Restore	

(7) / (3)

A	Q	M = 1101	
0000	0111	Initial values	
0000	1110	Shift	1
1101		Add	
0000	1110	Restore	
0001	1100	Shift	2
1110		Add	
0001	1100	Restore	
0011	1000	Shift	3
0000		Add	
0000	1001	$Q_0 = 1$	
0001	0010	Shift	4
1110		Add	
0001	$\boxed{0010}$	Restore	

(7) / (-3)

Fig.14: examples of signed and unsigned division.

Floating-point representation

Floating-point numbers are so called as the decimal or binary point floats over the base depending on the exponent value.

It consists two components.

- Exponent
- Mantissa

Example: Avogadro's number can be written as $6.02x10^{23}$ in base 10.

And the mantissa and exponent are 6.02 and 10^{23} respctivly.

But computer floating-point numbers are usually based on base two. So $6.02x10^{23}$ is approximately (1 and 63/64)$x2^{78}$ or 1.111111 (base two) x $2^{1001110}$ (base two)

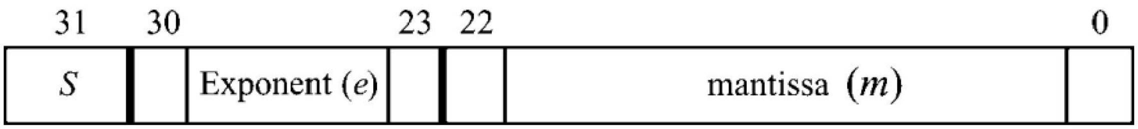


Fig. 15 IEEE-32 bit Floating-point number representation

According to Figure 15:

s = 1 bit sign

e = 8 bits of exponent

m = 23 bits of "mantissa" (the significant) (NOT the base; it's base two)

With some exceptions like:

- If the exponent is all ones (looks like 255), the number is a special value:
- if mantissa is all zeroes (0), value is is "+/- infinity" (depending on sign bit)
- else value is "NaN" ("not a number")

Floating Point Arithmetic Operation

Addition/Subtraction:

1. Before Addition/Subtraction two FP numbers their exponent must be equalized.
2. Compare the magnitude of the two exponents and make suitable alignment to the number with the smaller magnitude of exponent.
3. Perform the addition/subtraction.
4. Perform normalization by shifting the resulting mantissa and adjusting the resulting exponent.

Example 1: Add $1.100*2^5$ and $1.11*2^4$

- Align small exponent number is $1.11*2^4$ == $0.111*2^5$
- Now add two number to get result $10.011*2^5$
- Now normalize $1.0011*2^6$

Multiplication/ Division:

- Multiply/Divide mantissas
- Add/ Subtract exponents
- Normalize the rsult

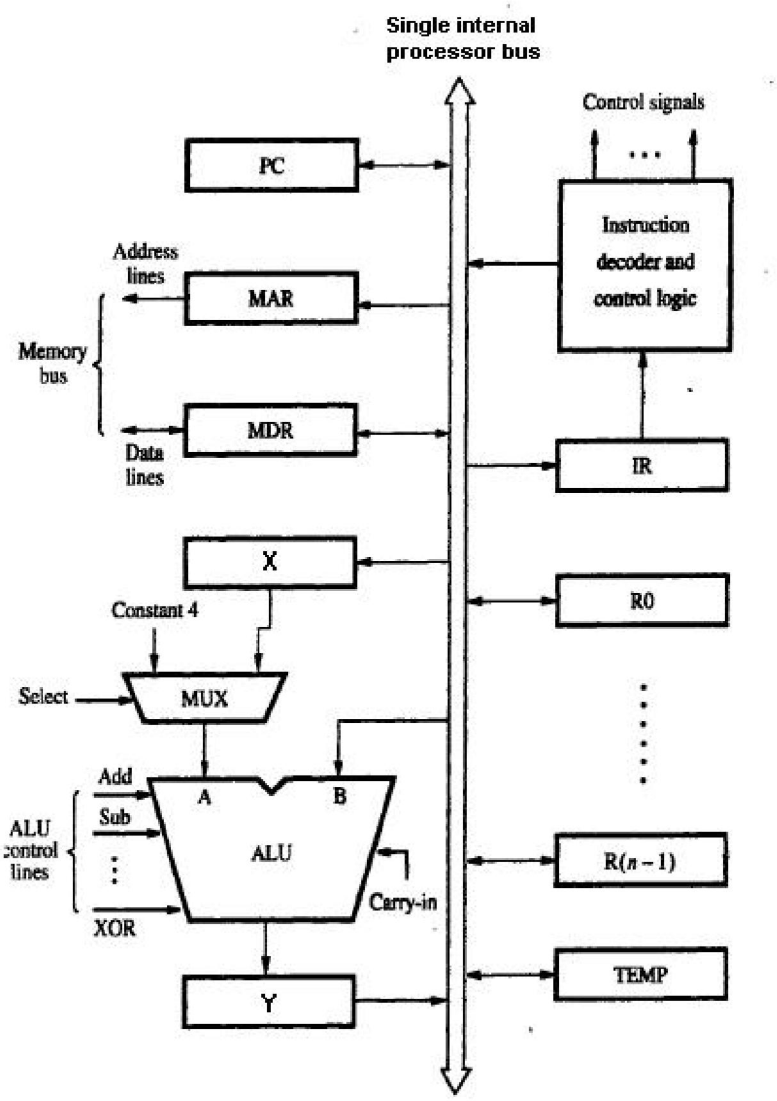
As an example:

$2.5*10^3$ X $0.25*10^2 = 0.625$ X $10^{(2+3)} = 6.25 * 10^5$

.

CPU ORGANISATION

Executing an instruction in cpu as sown in the fig. below :



Single Bus Organization

Fig.16 Single bus CPU connectivity

To execute an instruction in the fig.16, CPU performs the following steps

1) Send the content of PC to MAR for memory reading and wait till Memory function is completed.

MAR ß [PC]

2) Increment PC
PC ß [PC]+1

3) After memory read the instruction resides in MBR.

IR ß [MBR]

4) [IR] moves to decoder for decoding purpose.

5) Then the operation takes place according to the operand field of IR.

In above steps,

- step 1 to 3 is termed as instruction fetch phase.
- step 4 is known as decode phase
- step 5 is known as execute phase

Register transfer operations enable data transfer between various blocks connected to the common bus of CPU. Hence enabling the desired operations to be performed.

The following are the register transfer operations for some operations assuming CPU as single bus connected.

So to **Fetch an instruction** the steps are:

1. MAR à [PC], PC ß [PC+1]
2. Read Memory
3. Wait for MFC

To **Fetch data** the steps are:

1. MAR à [Rn / Address part of IR]
2. Read Memory
3. Wait for MFC

To **Store a data** in memory the steps are:

1. MAR ß [Rn / address part of instruction]

2. MBR ß [Rn]

2. Write Memory

3. Wait for MFC

The steps for addition of two registers R1 and R2 are:

1. Y ß [R1]
2. Z ß [R2] + [Y]
3. R_n ß [Z]

When a set of control signals are activated to perform an operation at a single clock cycle, it's known as **Control word.**

So the sets of control word for fetching an instruction from memory can be:

1. PC $_{out,}$ MAR $_{in,}$ Read, Select 1,Add,, Z $_{in}$

2. Z $_{out,}$ PC $_{in}$,WMFC

3. MDR$_{out}$, IR $_{in}$

Where PC$_{out,}$ MAR$_{in\ etc}$ are the control signals to close the PC-out switch, MAR-in switches so that the data can flow from PC and to MAR respectively.

Similarly the set of complete control words for instruction like ADD R1, R2, R3, where user desires that the content of R1 and R2 be added and stored at R3 , are:

1. PC $_{out,}$ MAR $_{in,}$ Read, Select 1,Add,, Z $_{in}$

2. Z $_{out,}$ PC $_{in}$,WMFC

3. MDR$_{out}$, IR $_{in}$

4. R$_{1\ out,}$ Y $_{in}$

5. R$_{3\ out,}$Select Y,Add, Z $_{in}$

6. Z$_{out}$, R$_{3\ in}$,End

Similarly to deviate from sequential execution, Branch instruction is used and the st of control words can be written as:

1. PC $_{out,}$ MAR $_{in,}$ Read, Select 1,Add,, Z $_{in}$

2. Z $_{out,}$ PC $_{in}$,WMFC

3. MDR$_{out}$, IR $_{in}$

4. PC$_{out}$, Y $_{in}$

5. Offset_field_of_IR $_{out,}$ Select Y,Add,Z $_{in}$

6. Z $_{out,}$PC $_{in,}$End

Introduction of Computer Memory :

What is the requirement of Memory:

A memory is just like a human brain. It is used to store data and instructions.

Memory can be characterized by the following points like:

- Speed
- Size
- Cost

Unit of Memory Size:

1 bit=the value of 0 or 1

8 bits = 1 byte

1024 byte =1 kilobyte

1024 kilobytes = 1 megabyte

1024 megabytes = 1 gigabyte

1024 gigabytes = 1 terabyte

1024 terabytes = 1 petabyte

Types of memory:

Memory is primarily of three types

- Cache Memory
- Primary Memory/Main Memory
- Secondary Memory

Cache Memory

Cache memory is a very high speed semiconductor memory which can speed up CPU. It acts as a buffer between the CPU and main memory. It is used to hold those parts of data and program which are most frequently used by CPU. The parts of data and programs are transferred from disk to cache memory by operating system, from where CPU can access them.

Advantages

The advantages of **cache memory** are as follows:

- § Cache memory is faster than main memory.
- § It consumes less access time as compared to main memory.
- § It stores the program that can be executed within a short period of time.
- § It stores data for temporary use.

Disadvantages

The disadvantages of cache memory are as follows:

- § Cache memory has limited capacity.
- § It is very expensive.

Primary Memory (Main Memory)

Primary memory holds only those data and instructions on which computer is currently working. It has limited capacity and data is lost when power is switched off. It is generally made up of semiconductor device. These memories are not as fast as registers. The data and instruction required to be processed reside in main memory. It is divided into two subcategories RAM and ROM.

Types of RAM:

- Static RAM
- Dynamic RAM

Types of ROM:

- ROM
- PROM
- EPROM

- EEPROM

ROM Vs RAM

There is one major difference between a ROM and a RAM chip.

- A ROM chip is non-volatile storage and does not require a constant source of power to retain information stored on it. When power is lost or turned off, a ROM chip will keep the information stored on it. So for permanent storage, ROM is used.
- In contrast, a RAM chip is volatile and requires a constant source of power to retain information. When power is lost or turned off, a RAM chip will lose the information stored on it.
- A ROM chip is used primarily in the start up process of a computer, whereas a RAM chip is used in the normal operations of a computer after starting up and loading the operating system.
- Writing data to a ROM chip is a slow process, whereas writing data to a RAM chip is a faster process
- A RAM chip can store multiple gigabytes (GB) of data, up to 16 GB or more per chip; A ROM chip typically stores only several megabytes (MB) of data, up to 4 MB or more per chip

Advantages of Main Memory

These are semiconductor memories

- It is working memory of the computer.
- Faster than secondary memories.
- Cheaper than Cache memory.

Disadvantages of Main Memory:

- Volatile when power goes off.
- High cost as transistors are used.
- Usually size is less than secondary memory.

Secondary Memory

This type of memory is also known as external memory or non-volatile. It is slower than main memory. These are used for storing data/Information permanently. CPU directly does not access these memories instead they are accessed via input-output routines. Contents of secondary memories are first transferred to main memory, and then CPU can access it. For example : disk, CD-ROM, DVD etc.

Advantages of Secondary Memory

- These are magnetic and optical memories
- It is known as backup memory.
- It is non-volatile memory.
- Data is permanently stored even if power is switched off.
- It is used for storage of data in a computer.

Disadvantages of Secondary Memory

- Computer doesn’t deal with secondary memory at the beginning of execution.
- Slower than primary memories.

Memory Hierarchy

Ideally we need fast, large and cheap memory. But unfortunately it’s not possible to get all the three simultaneously. So a various types of memory like above having different characteristics are used. for different purposes combinedly, which creates a hierarchy of memory module wile being used in computer. This is depicted in the fig. 17.

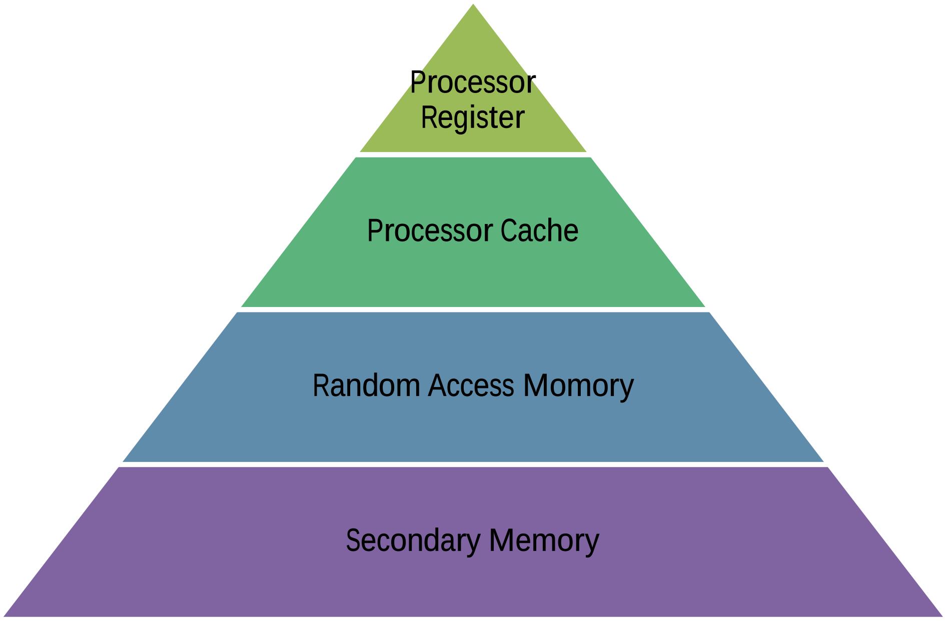


Fig. 17: Memory Hierarchy

Assignments on Module-1.

1. Write the control words for the instruction MUL R4 R5 R6 where user wants content of R4 and R5 be added and stored at R6 in CPU 3-bus connectivity.
2. Perform the following operation using 2's complement form.

   i. 3 – (-7) ii. -7 / 3 iii. -3 X -7
3. Convert 65.55 to IEEE 64 bit format.
4. Enlist the advantages and disadvantages of Von Neumann's computer.
5. Write advantages and disadvantages of ach of the fixed point number representation technology.