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Programmable spintronics logic device based on a magnetic tunnel junction element

Jianguo Wang, Hao Meng, and Jian-Ping Wang[a)]
The Center for Micromagnetics and Information Technology (MINT), Department of Electrical and Computer Engineering (ECE), University of Minnesota, 200 Union Street SE, Minneapolis, Minnesota 55455

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A programmable spintronics logic device was designed and fabricated based on a single pinned magnetic tunnel junction (MTJ) element. In this work, a current input line C passing through the MTJ element itself was introduced. Two separated input current lines (A and B) could switch the magnetization of the pinned layer under the heat assistance from line C. Full logic functions (AND, OR, NAND, NOR, XOR, and XNOR) can be realized based on a normal pinned and a synthetic pinned MTJ element. A Wheatstone bridge was engineered to read this single MTJ element logic device. MTJ elements with 1 μm^2 and normal pinned structure: (Ta 30 Å/NiFe 40 Å/MnIr 35 Å/CoFe 30 Å/(Al 7 Å)+oxidation/CoFe 30 Å/NiFe 40 Å/Ta 200 Å), have low resistance of 6.3 Ω and high resistance of 7.2 Ω, which gives the magnetoresistive (MR) ratio of 14%. Approximately a 3-mV output difference is obtained between logical 1 and 0. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1857655]

I. INTRODUCTION

Programmable spintronics logic devices show many potential advantages compared to traditional semiconductor logic devices, such as nonvolatility, rapid, unlimited reconfigurable variations, and low-power consumption. Recently, several ideas have been proposed to implement logic functions based on a single unpinned magnetoresistive (MR) element or several pinned MR elements.[1–14] The variation of switching thresholds of two magnetic layers makes it impossible to implement a real logic device based on single unpinned MR element.[4,5] Pinned MR elements are successfully used for magnetic read head and magnetic random access memory,[15,16] but they result in low density because several pinned MR elements are needed for each device.[10,11] In this work, a spintronics logic device based on a single pinned magnetic tunnel junction (MTJ) element was fabricated and tested. By introducing a current input line passing through the MTJ itself and using the principle of thermal magnetic writing, both free and pinned layers can be logic active so that the six logic functions (AND, OR, NAND, NOR, XOR, and XNOR) can be realized.

II. DEVICE DESIGN AND OPERATION

The two resistance states of MTJ (high and low) can be identified with a logical 1 and 0, respectively. Figure 1(a) shows the schematic of a MTJ spintronics logic element. Two input lines, A and B, are operated with positive and negative currents identified with a logic value of 1 or 0, respectively. The magnetic field generated at the free layer by the input line A or B points to the right and left for positive and negative currents, respectively. For writing a bit, the magnetic field generated by a current in either line A or B in Fig. 1(a) is sufficient to rotate the magnetization direction of the free layer. The magnetization direction remains when the current is turned off. Input C is operated with current (logical 1) or without current (logical 0). With current, the input C generates heat to raise the temperature of the MTJ cell to the pinned layer blocking temperature, and pinned layer magnetization direction can be reversed under the magnetic field generated from inputs A and B.[17] Without the current in the input C, the pinned layer keeps its magnetization direction regardless of magnetic field. As shown in Fig. 1(b), a MTJ element with a normal-pinned structure (Ta 30 Å/NiFe 40 Å/MnIr 35 Å/CoFe 30 Å/Al 7 Å +oxidation/CoFe 30 Å/NiFe 40 Å/Ta 200 Å) can realize five logic gates (AND, OR, NAND, NOR, and XOR). And as

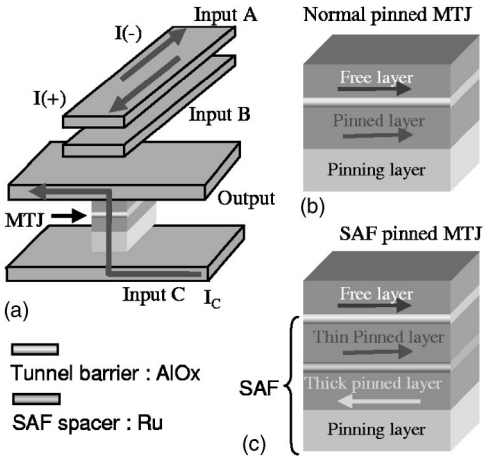

FIG. 1. (a) Schematic of a programmable spin-logic device based on a single MTJ element with two independent input lines A and B, a third input line C, and an output line. (b) MTJ with a normal bottom pinned structure for logic gates (AND, OR, NAND, NOR, and XOR). (c) MTJ with a synthetic bottom pinned structure for logic gates and (AND, OR, NAND, NOR, and XNOR).

[a)]Author to whom correspondence should be addressed; electronic mail: jpwang@ece.umn.edu

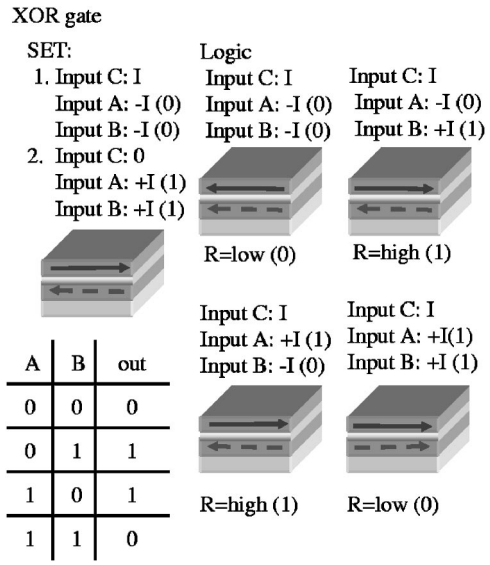

FIG. 2. Principle of XOR gate operation and the inset is its lookup table.

TABLE I. Operation principle for spin-logic gates (AND, OR, NAND, and NOR) based on a single normal bottom pinned MTJ element.

Set step	input A	Input B	Input C	After logic	Out
AND	$+I(1)$	$+I(1)$	0	⇄	1
	$+I(1)$	$-I(0)$	0	⇇	0
⇇	$-I(0)$	$+I(1)$	0	⇇	0
	$-I(0)$	$-I(0)$	0	⇇	0
OR	$+I(1)$	$+I(1)$	0	⇄	1
	$+I(1)$	$-I(0)$	0	⇉	1
⇉	$-I(0)$	$+I(1)$	0	⇉	1
	$-I(0)$	$-I(0)$	0	⇇	0
NAND	$+I(1)$	$+I(1)$	0	⇉	0
	$+I(1)$	$-I(0)$	0	⇄	1
⇄	$-I(0)$	$+I(1)$	0	⇄	1
	$-I(0)$	$-I(0)$	0	⇉	1
NOR	$+I(1)$	$+I(1)$	0	⇉	0
	$+I(1)$	$-I(0)$	0	⇉	0
⇉	$-I(0)$	$+I(1)$	0	⇉	0
	$-I(0)$	$-I(0)$	0	⇄	1

detailed in Fig. 1(c), a MTJ element with a synthetic pinned layer structure can realize five logic gates (AND, OR, NAND, NOR, and XNOR). Using XOR as examples, we describe their operation in detail.

The XOR gate design is shown in Fig. 2, in which the MTJ element has a normal pinned structure. The dashed and solid arrows represent the pinned (M_p) and free layer magnetization (M_f), respectively. The operation is performed in two steps. The first step, named "SET," sets the MTJ element to an initial logic state, and the second step, named "Logic," is the step in which the MTJ element output depends on the inputs. For the XOR gate, the initial magnetization state of the free layer should point to the right and the pinned layer to the left. During SET step, the inputs A, B, and C are 0, 0, and 1 initially. Both M_f and M_p will point to the left. The inputs A, B, and C are then set as 1, 1, and 0, respectively. Only the M_f is reversed to the right eventually. For the Logic step, the input C is set as 1. When inputs A and B are both 0 or 1, both M_f and M_p are parallel to the left or the right, respectively, the resistance of MTJ is low, which presents the logical 0. When either of inputs A and B is 1 and the other one is 0, the magnetic fields cancel each other, the magnetization direction of both the free and pinned layers keep unchanged, and the resistance is high, which output the logical 1. The inset table of Fig. 2 is the logic function table for the XOR gate. The other four gates functions (AND, OR, NAND, and NOR), initial states, and logic operations are described in Table I.

To implement the above ideas, a Wheatstone bridge was engineered to read this single MTJ element logic device, as shown in Fig. 3(a). Three of the four MTJ elements in Fig. 3(a) function as resistors with low resistance while the fourth is the logic device. When the active MTJ cell is with low (logical 0) or high (logical 1) resistance, the bridge output is with low (logical 0) or high (logical 1) voltage, respectively. Figure 3(b) shows the spintronics logic chip made on a Si wafer; there are four logic devices in each die. MTJ cells with a 1-μm^2 size have normal pinned structure, as stated above. For input A, currents of −70 and +55 mA are identified as logical 0 and 1, and for input B, currents of −40 and +30 mA are identified as 0 and 1. For input C, currents of 0 and 50 mA are identified as 0 and 1, respectively. A magnetic field of 0.9 and 1.6 Oe/mA are generated at the free layer from inputs A and B, respectively. When input A ≠ B, a magnetic field of 15 Oe pointing to the left is generated at the free layer, which is needed to cancel the vortex field generated by input C that slightly changes the pinned layer magnetization direction for the XNOR or XOR logic operation.

Figures 3(c) and 3(d) are the minor MR loops of the active MTJ element measured under the magnetic field generated from inputs A and B. From the curves, the coercivity of the free layer is around 50 Oe. The diamond curves are for the MTJ element with the pinned layer magnetization pointing to the right that is set by inputs A, B, and C with currents of −70, −40 and 50 mA, respectively. The square curves are for the MTJ element with the pinned layer magnetization pointing to the right that is set by inputs A, B, and C with currents of 55, 30, and 50 mA, respectively. The MTJ element had a low resistance of 6.3 Ω and a high resistance of 7.2 Ω, which gives the MR ratio of 14%.

Figure 3(e) shows the logic gate of XOR and OR operations. A voltage of 1 V is applied across the Wheatstone bridge. The average lead and contact resistance of each branch of the bridge was 45 Ω, and the voltage drop over each MTJ element was 63 mV. The first step is the XOR gate SET. By setting inputs A, B, and C as 0, 0, and 1 and followed by 1, 1, and 0, the magnetization directions of the pinned layer and the free layer are antiparallel. The logic-active MTJ element has high resistance, and the bridge has an output of 16.4 mV (logic 1). The second step is the XOR gate Logic. When inputs A, B, and C are 1, 1, and 1, the magnetization directions of the free layer and pinned layer become parallel. The logic-active MTJ element has an low resistance and the bridge has an output of 13.2 mV (logic 0). The third step is the OR gate SET. By setting inputs A, B, and C as 0, 0, and 1 and followed by 1, 1, and 0, the mag-

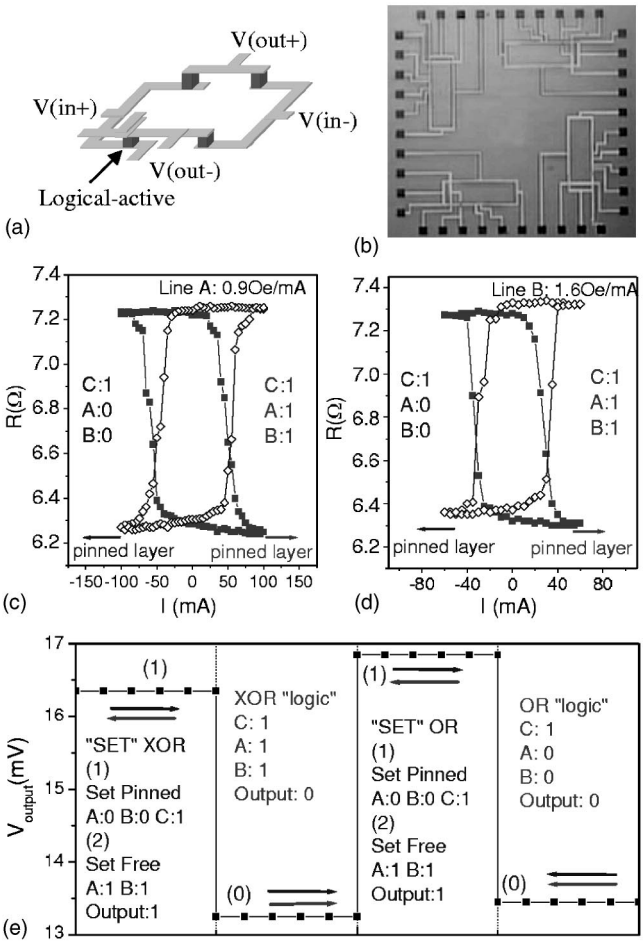

FIG. 3. (a) Schematics of Wheatstone bridge-type spin logic with one logic-active MTJ element. (b) Optical micrograph of spin-logic circuit made on a Si wafer with four Wheatstone bridge-type spin logic in each die. (c) and (d) are minor MR loops of active MTJ element operated under magnetic field generated from inputs A and B, respectively. (e) XOR and OR gate operations.

netization directions of the pinned layer and free layer are antiparallel. The logic-active MTJ element has high resistance and the bridge has an output of 16.8 mV (logic 1). The fourth step is the OR gate Logic. When inputs A, B, and C are 0, 0, and 1, the magnetization directions of the free layer and pinned layer become parallel. The logic-active MTJ element has low resistance and the bridge has an output of 13.2 mV (logic 0). The 13.2-mV voltage is the offset of the bridge. About 3-mV output difference is obtained between the logical 1 and 0. The output signal could be improved by increasing the MR ratio. For example, if we use MgO as the barrier layer, the MR ratio could be up to 220% at room temperature.[18,19] This will greatly increase the logic device output signal. Further work is ongoing in our lab to improve the logic device performances.

III. CONCLUSION

The programmable spintronics logic devices based on a single pinned MTJ element was designed and fabricated in this work. By introducing a current input line passing through the MTJ itself and using the principle of thermal-assisted magnetic writing, six logic functions (AND, OR, NAND, NOR, XOR, and XNOR) were realized on a single MTJ cell for the first time.

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