Week 2: Assignment Solutions

1. The binary equivalent of 45.625 is 101101.101 .

   Solution: 45 in binary is 101101, and .625 in binary is .101

2. The decimal equivalent of 10110.001 is 22.125.

   Solution: 10110 in decimal is 22, and .001 in binary is .125

3. The hexadecimal equivalent of 11010011001010100
   a. 1A654
   b. C32A0
   c. 8A654
   d. None of the above

   Solution: (a) The bits are divided in groups of 4 from the right, and we add leading zeros as required. Thus,

   0001 1010 0110 0101 0100

4. The maximum unsigned binary number that can be represented in 12 bits is 4095 .

   Solution: The range of numbers that can be represented in n-bit unsigned representation is 0 to 2^n-1. For n=12, the maximum number is 2^{12}-1 = 4095.

5. Which of the following are true for n-bit sign number representation?
   a. The minimum and maximum number that can be represented in sign magnitude is – (2^{n-1} - 1) and + (2^{n-1} - 1)
   b. The minimum and maximum number that can be represented in one's complement is – 2^{n-1} and + (2^{n-1} - 1)
   c. The minimum and maximum number that can be represented in two's complement is – 2^{n-1} and + (2^{n-1} - 1)
   d. None of the above

   Solution: ((a) and (c)) Follows from the definition of sign magnitude, 1's complement and 2's complement representations. For 1's complement, the smallest number is – (2^{n-1} - 1) .

6. In two's complement representation -6 can be represented by 1010 in four bits. The representation of -6 in 8-bit will be 11111010 .

   Solution: We need to pad 1's in the beginning. Hence 11111010 in 2's complement is equivalent to $-2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 0 \times 2^2 + 2^1 + 0 \times 2^0$ which is (-128 + 64 + 32 + 16 + 8 + 2) = -128 + 122 = -6.

7. There are 50 registers, and total 55 instructions available in a general-purpose computer. The computer allows only 2-address instructions, where one operand can be a register and another can be a memory location. The memory is byte addressable with 64KB (Kilo bytes) in size. The minimum number of bits to encode the instruction will be 28 .

Solution:

Total registers = 50; hence number of bits required to represent one register will be 6 as $50 < 2^6$.

Total instructions = 55; hence again 6 bits will be required to represent an instruction.

Total memory = 64KB = $2^6 2^{10}$B; hence 16 bits will be required to represent a memory location.

An instruction has two parts, Opcode and Operand. In this problem there are only 2-address instructions, out of which one is register operand and other is memory operand.

Hence total bits will be: 6 (opcode) + 6 (register operand) + 16 (Memory operand) = 28 bits

8. Registers R1 and R2 contain data values 1800 and 3800 respectively in decimal, and the word length of the processor is 4 bytes. The effective address of the memory operand for the instruction "ADD 100(R2),R6" will be 3900 .

   Solution: 100 + content of R2 = 3900.

9. Registers R1 and R2 contain data values 600 and 800 respectively in decimal, and the word length of the processor is 4 bytes. The effective address of the memory operand for the instruction "LOAD R5,10(R1,R2)" will be 1410 .

   Solution: 10 + content of R1 + content of R2 = 1410.

10. Consider a processor with 64 registers and an instruction set of size 12. Each instruction has 5 distinct fields, namely opcode, two-source register identifiers, one destination register identifier, and a 12-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion (i.e. from an address that is a multiple of 4). If a program has 100 instructions, the amount of memory consumed by the program is 800 bytes.

    Solution: Each instruction has 5 distinct fields:

    Opcode, Register1, Register2, Register3, 12-bit immediate value

    Total instructions = 12; hence it requires 4 bits

    Total registers = 64; hence 6 bits are required to specify the register.

    Immediate value = 12-bits

    Total length of an instruction: 4 + 6 + 6 + 6 + 12 = 34 bits, i.e. slightly more than 4 bytes.

    Hence each instruction will require 8 bytes to make it byte aligned. Hence 800 bytes will be required.

11. For a computer based on 3-address instruction formats, each address field is used to specify which of the following?
    (S1) A memory operand
    (S2) A processor register
    (S3) An implied accumulator register

a. Either S1 or S2
b. Either S2 or S3
c. Only S2 and S3
d. All of S1, S2 and S3

Solution: (a) An address can specify either a memory operand or a processor register. We do not refer to an implied operand by an address.

12. Which of the following statements are false for MIPS 32 register set?
    a. Register R0 always contains the value 0.
    b. Any register other than R0 can be used for register indirect addressing.
    c. Any register other than R0 can be used to hold the return address for function calls.
    d. R31 is a special register used as stack pointer.

    Solution: ((c) and (d)) Only R31 can be used to store the return address. There is no specific register designated as the stack pointer.

13. The MIPS code for A = B+C where B is loaded in register $S2 and C is loaded in register $S3 is
    a. ADD $S1, $S2, $S3
    b. ADDI $S3, $S2, $S1
    c. ADD $S3, $S2, $S1
    d. None of the above

    Solution: (a) The content of registers $S2 and $S3 are added and stored in register $S1.

14. In MIPS32, to fetch a 32-bit word from memory in a single cycle, the word has to be stored from memory location:
    a. 0018H
    b. 0019H
    c. 001AH
    d. 001BH

    Solution: (a) For fetching a word in a single cycle it should be fetched from a memory location which is multiple of 4; and hence here it will be 0018H.

15. The MIPS instruction BNE $S0, $S1, Label means:
    a. If $S0 is not equal to $S1 then do not branch to location Label
    b. If $S0 is not equal to $S1 then branch to location Label
    c. If both $S0 and $S1 are not equal to 0 then branch to location Label
    d. None of the above

    Solution: (b) Branch Not Equal (BNE) means if $S0 is not equal to $S1 then branch to location Label.